Design and FPGA Implementation of Digital Frequency Modulation Receiver

Khadija Shazly[*1], Mohamed E. Ghoneim[2], Sunil Kumar[3]

[1] Faculty of Computer and Information, Mansoura university, Egypt
[2]Department of Mathematical Sciences, Faculty of Applied Science, Umm Al-Qura University, 21955 Makkah, Saudi Arabia
[3] School of Computer Science, University of Petroleum and Energy Studies, Dehradun, 248001, India

Emails: khadijashazly@students.mans.edu.eg; meghoneim@uqu.edu.sa; skumar@ddn.upes.ac.in

Abstract

In this paper, we introduce the design of a digital frequency modulation receiver using FPGA. The main component in the design is digital phase locked loop (DPLL) which compensate any changes between the frequency and phase of the input modulated signal and the frequency and phase of numerically controlled oscillator. The input to the receiver is 8-bit represents the sampled discrete time signal from the analog modulated received frequency modulation signal. The receiver is designed using Xilinx system generator and implemented on the FPGA board (Xilinx Vitrex-7 XC7VX550t board), works with 350 MHz and consumes 120 mW.

Keywords: Frequency modulation; Digital phase locked loop; field programmable gate array.

1. Introduction

Nowadays all fields of wireless communication, networks, satellite and mobile communications systems move from analog to digital communications due to reliability, simplicity, efficiently, and low power consumption. The block diagram of digital communication system is indicated in Figure 1.

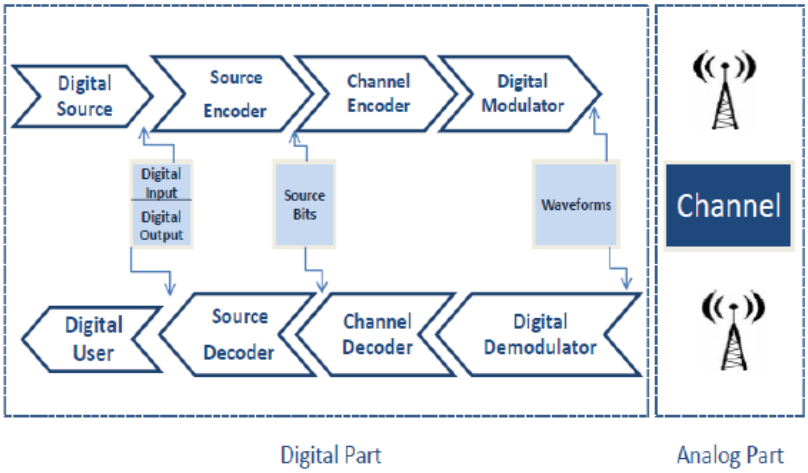

Figure 1: A Digital communication system

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

Both digital and analogue parts make up the digital communication system. The digital components include the digital source/user, encoder/decoder, encoder/decoder for the channel, and the modulator/demodulator for the digital signal. Transmitter, receiver, channel models, and noise models make up the analogue portion [1]. An electronic medium, specifically a computer, will be conveying the message. The digital information is received by the source encoder, which then makes the necessary preparations for the source messages. The channel encoder converts a given symbol sequence into another symbol sequence. The digital modulator acts as an interface between the communication channel and the encoder, receiving the binary information at the encoder's output. The modulator's primary function is to convert the discrete symbols into a channel-transmittable analogue waveform. Reverse signal processing takes place at the receiver. Between the sender and the receiver, there exists a physical conduit called a channel. No matter what medium is utilised, the signal is contaminated by noise [2]. Receiving it, the connection between the source and the target of a transmission is called a channel. No matter what medium is utilised, the signal will be distorted by noise. A digital communication system's primary function is to carry digital information between a sender and a recipient. It is possible for the signals to be distorted as they travel between the two nodes because of the imperfection of the channel. Whether it's the frequency, the phase, or the amplitude of a sinusoidal carrier, digital data is sent from sender to receiver in this way. To accomplish this, a modulator is used at the sending end on impose the physical change to the carrier, and a demodulator is used at the receiving end to detect the modulation. Modulation of the amplitude, phase, or frequency of a signal during transmission is known as digital modulation. The bandwidth of the transmitted signal is set by the transmission rate of the symbols, which the modulation technique compressed into relatively small bundles. For a given signal bandwidth, a higher data rate can be achieved by increasing the number of bits per symbol. However, the needed received signal to noise ratio (SNR) for a particular target Bit Error Rate (BER) increases as the number of bits per symbol increases [3-4]. Figure 2 depicts the frequency modulation (FM) technique or process, which encodes information onto a signal (analogue or digital) by adjusting the carrier wave frequency to match that of the modulating signal [5-7]. To put it simply, a modulating signal is any information or message that must be sent by electronic signal.

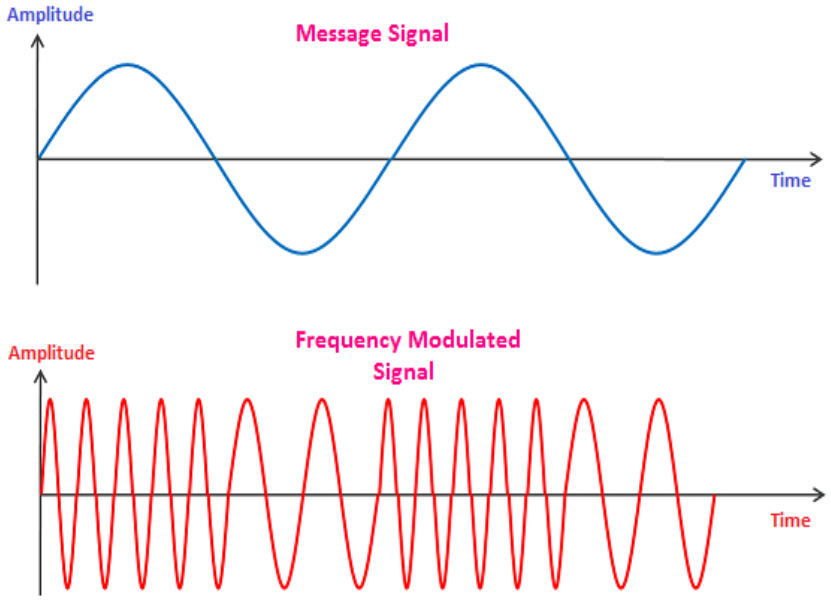

Figure 2: Frequency modulation technique

Similar to amplitude modulation, in frequency modulation an input signal is used to alter a carrier signal. With FM, on the other hand, the amplitude of the modulated signal is maintained or kept constant. There is typically a need for a bandwidth of 200 kHz or more and a frequency modulation index of greater than 1. FM radio transmits at extremely high frequencies, often between 88 and 108 MHz. In order to receive high-quality signals with great sound quality, there exist sophisticated circuits with an endless number of sidebands.

In contrast, broadcast stations in the VHF range (88.5 MHz - 108 MHz) frequently employ substantial quantities of deviation (75 kHz). Broadband FM is the term for this type of transmission (WBFM). These signals allow for

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

high-quality broadcasts, but they take up a lot of bandwidth. Each wide-band FM transmission typically has a maximum frequency of 200 kHz.Conversely, bandwidth consumption is low for communications. However, deviation figures about 3 kHz are commonly used in narrowband FM (NBFM). Further, two-way radio communications are the primary use of narrow-band FM [5]. Frequency modulation finds most of its uses in radio transmission. Since the signal-to-noise ratio is improved, it is a significant benefit in radio transmission. That is to say, there is minimal interference with radio waves as a result. Because of this, FM is widely used by radio stations to broadcast music. It is also used in radar, telemetry, and seismic prospecting; EEG; various radio systems; music synthesis and video-transmission instruments; and so on. Frequency modulation has a number of advantages over other types of modulation for use in radio transmission. Due to its higher signal-to-noise ratio, it is more effective at filtering out RF interference than an AM signal of the same strength. Because of this, FM radio has become the de facto standard for music broadcasting. In this work, we show how to create a digital FM receiver with an FPGA. This study delves into the mathematical model, the hardware model, and the outcomes of the implementation.

2. FM Receiver Design

The block diagram of architecture is shown in figure 3. It simply consists of digital phase lock loop (DPLL) and low pass filter (LPF) [8-13].

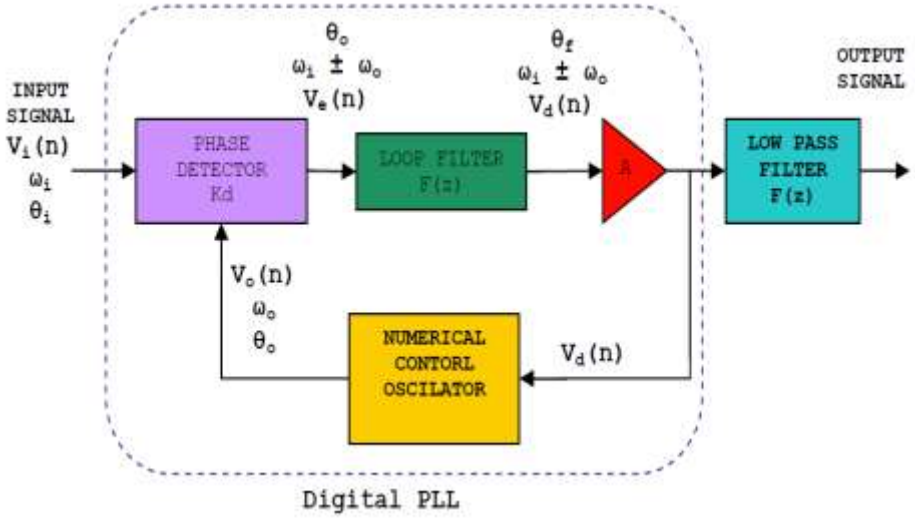

Figure 3: Frequency modulation receiver

The function of phase detector inside DPLL is to perform multiplication between input signal and the signal of NCO to determine the phase difference between both of them. The received input signal is:

$$v_i(n) = \sin(\omega_i n + \theta_i) \quad (1)$$

Where

ω_i: the input radian frequency

θ_i: the input phase

$$v_o(n) = \cos(\omega_i n + \theta_o) \quad (2)$$

Where

θ_0: the generated phase of NCO signal

Output of phase detector is product of these two signals, using familiar trigonometric identity we obtain

$$v_d(n) = \frac{k_d}{2}[\sin(2\omega_i n + \theta_i + \theta_0) + \sin(\theta_i - \theta_0)] \quad (3)$$

Where

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

k_d: phase detector gain

The term $(\frac{k_d}{2}[\sin(2\omega_i n + \theta_i + \theta_0])$ is high frequency component and have to be removed by the loop filter inside DPLL. While the term $(\frac{k_d}{2}[\sin(\theta_i - \theta_0])$ represents phase difference. The block diagram of phase detector is shown in Figure 4.

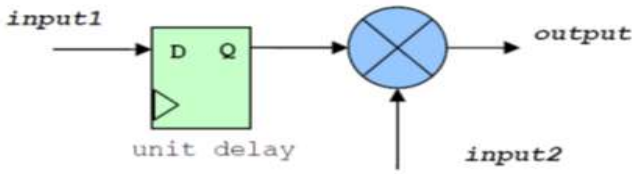

Figure 4: Phase detector

The NCO's output is displayed at input2, while the modulated input signal is shown at input1. Both of these are in the 2's complement format. Following synchronisation via the unit delay, we multiply the values of the inputs, with input1 serving as the multiplicand and input2 acting as the multiplier, yielding a 16-bit result; we then scale this value by discarding the eight most significant bits. Since the usage of a simple signed arithmetic multiplier operation would result in excessive space utilisation, we employ Booth's Multiplication algorithm instead which shows in details in figure 5 [14-16].

```
2's complement of multiplicand 10111 is 01001

9 8 7 6 5 4 3 2 1 0  bit weighting
        1 0 1 1 1  multiplicand (-9)
        1 0 0 1 1  multiplier (-13)        first 1
                                           first 0
                                           second 1
---------------------
0 0 0 0 0 0 1 0 0 1  1st multiplier bit 1 - subtract (add 2' complement)
0 0 0 0 0 0 0 0 0    2nd multiplier bit also 1 - no change so no add/subtract
1 1 1 1 0 1 1 1      3rd multiplier bit changes to 0 so add. Note sign extension
0 0 0 0 0 0 0        4th multiplier bit also 0 - no change so no add/subtract
0 0 1 0 0 1          5th multiplier bit changes to 1 so subtract (add 2's compl)
---------------------
0 0 0 1 1 1 0 1 0 1  product (+117)
---------------------
Note the overflow of adding the partial product into 11th bit (bit weighting 10) of the
product is ignored as it represents the original sign bit of the multiplier.
```

Figure 5: Explanation of Booth multiplication algorithm

Figure 6 shows the block diagram of a first order loop filter used in the receiver system.

The transfer function of the loop filter is

$$H(z) = \frac{z^{-1}}{1-0.93\,z^{-1}} \qquad (4)$$

The pole of the system lies inside the unit circle which means stability of the system.

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

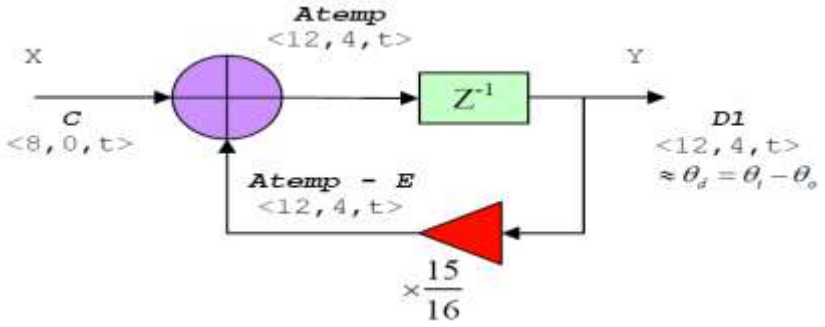

Figure 6: Low pass filter structure

Numerical Controlled Oscillator (NCO) task is to keep the input frequency and phase synchronized with the generated frequency and phase of NCO by changing the generated frequency of NCO to match any changes in the input frequency and phase. NCO block diagram shown in figure 7 [17-20].

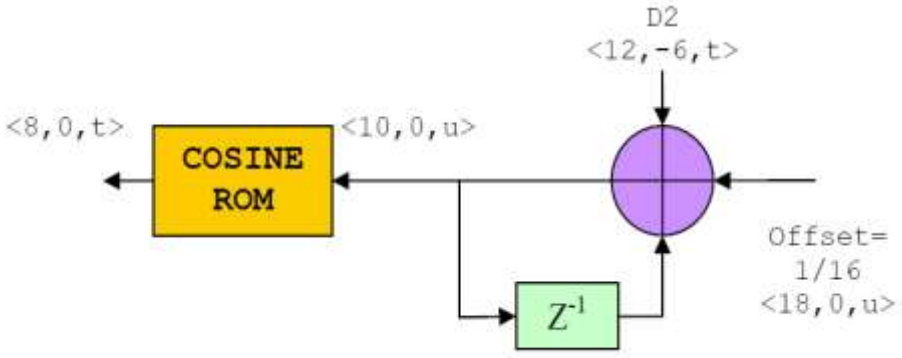

Figure 7: Block diagram of NCO

Assuming a system clock frequency of 16 MHz and a free running frequency of 1 MHz for the NCO in question, we get 16 samples per cycle. NCO is required to provide output equal to free running frequency when input is zero. The offset must be 1/16. Higher frequency results from higher input, and vice versa. The system is a straightforward integrator that adds up the input value and converts it to a set of cosine ROM values. We only need to define the first quarter with 257 numbers because a cycle can be broken down into four quarters. The second and third quarters are carbon copies of the first, with the opposite sign applied. The final component of the architecture is finite impulse filter with 16 tap as shown in figure 8. The main function of the filter is to smooth the output signal.

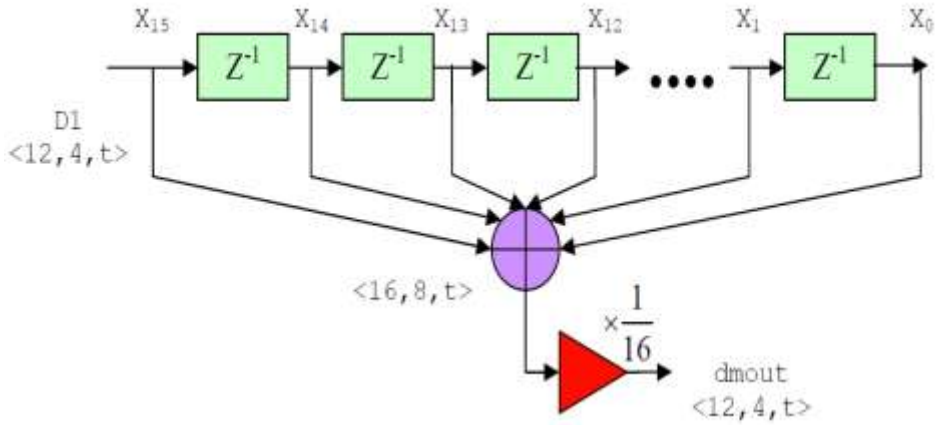

Figure 8: Block diagram of FIR filter

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

Figure 9 is a schematic depicting the whole circuitry of a Digital FM receiver. Having been subjected to no external signals whatsoever.

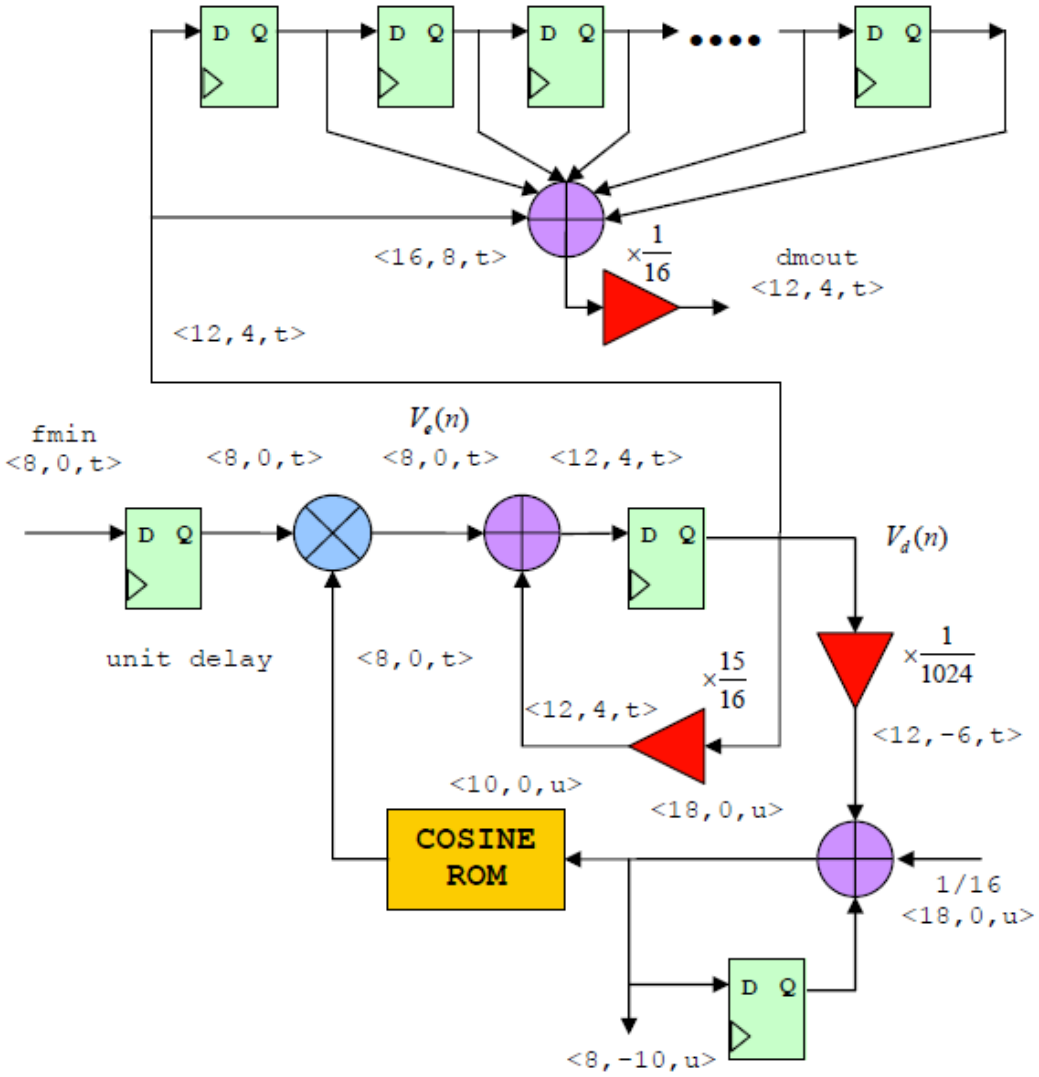

Figure 9: Digital FM Receiver system

Afterwards, the NCO's control terminal receives the filtered and amplified. In PLL, the NCO will lock to the input signal if the input frequency. When the NCO is locked in, the frequency is the same as the input signal within a defined phase difference [21]. This results in a net phase difference is

$$\theta_2 = \theta_i - \theta_o \qquad (5)$$

generates the correction error voltage that locks the NCO frequency to the input signal frequency, allowing the PLL to continue operating. Once locked, the PLL can follow the frequency variations of the input signal and serve as an FM demodulator in a receiver system thanks to the system's inherent self-correcting abilities. The output of PD produces the sum and difference frequencies ($\omega_i \pm \omega_0$). The NCO will replicate the input frequency while the loop is locked, resulting in a difference frequency component of (ω_i-ω_0). 0, hence there is no AC component at all in the phase comparator's output. In order to get rid of the accumulated frequency (ω_i+ω_0), the loop filter is applied. but the DC part is transmitted and amplified before being sent back to the NCO. The transient and steady-state behaviour of the all-digital PLL system can be analysed with the help of a mathematical model. Figure 10 indicates block diagram of the architecture in the s-domain

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

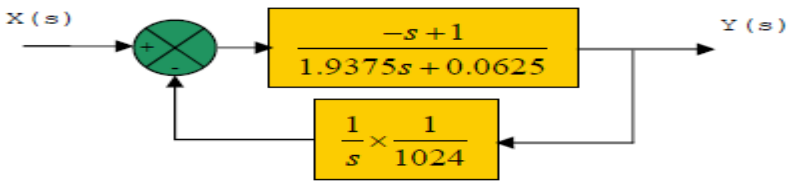

Figure 10: Block diagram of PLL system in analyzing transient response

Because of the need to store energy, transient responses are present when an input is made to a physical control system before the system settles into a steady state [22-23].

The system's transfer function is

$$H(s) = \frac{-s^2+s}{1.94s^2+0.06s+0.00089} \qquad (6)$$

To a stability test using a signal that represented a single frequency step at a fixed phase, mimicking the actual input signal, which was FM modulated. The unit step response curve for the system can be plotted in MATLAB, as illustrated in figure 11. Overshoots at the transitory state show that the system is stable.

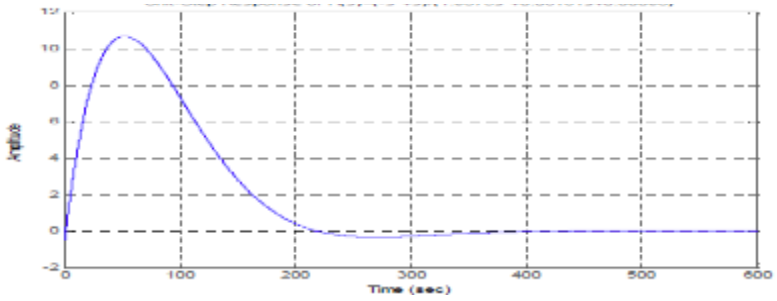

Figure 11: Unit step response for PLL

3. Simulation Results

In figures 12 and 13, we see the simulated waveforms for a fully digital FM receiver circuit when it is exposed to square wave modulated data and a triangular wave. According to the transmitted data, the FM modulated waveform is displayed in the first row. The NCO output can be seen in the second row, while the phase detector (multiplier) output can be seen in the third row. The demodulated output may be found in the fifth row, while the accumulator output can be found in the fourth. Since the phase synchronisation is in the convergence phase and then the system is stable at the beginning of the simulation phase, the demodulated output overshoots [24-27].

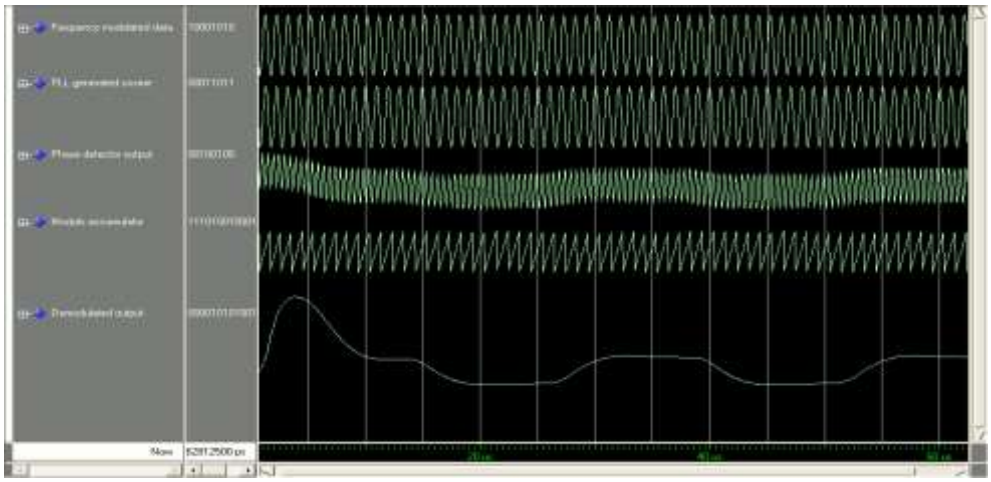

Figure 12: Simulation waveform of the circuit, subjected to square wave modulated input signal

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

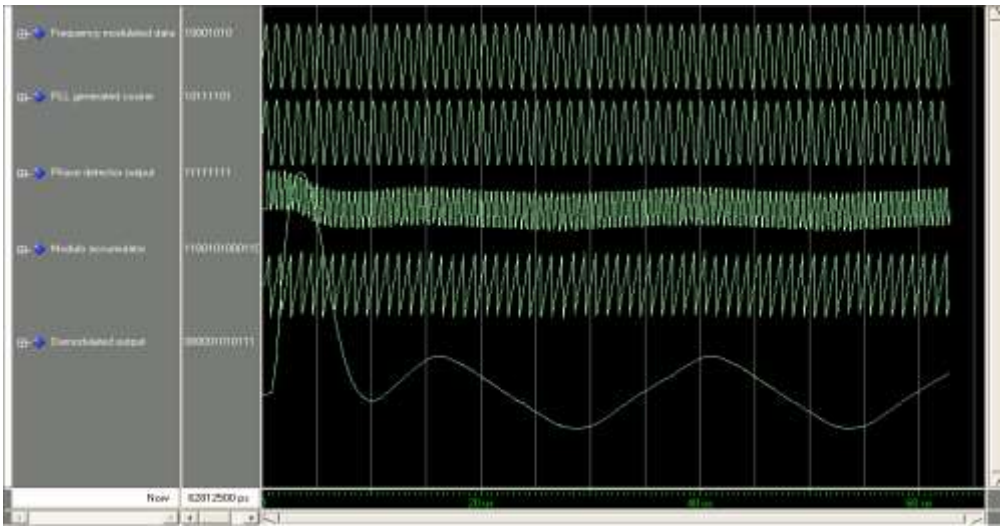

Figure 13: Simulation waveform of the circuit, subjected to square wave modulated input signal

4. Hardware Results

The receiver architecture is implemented using FPGA of type Xilinx Vitrex-7 XC7VX550t board. [28-33].The device utilization report, which indicates how much resources of the FPGA board are used to implement the FM receiver is shown Table 1.

Table 1: FPGA consumed resources

Component	Proposed	Available
slice flip flops	98	33280
4 input LUTs	189	33280
bonded IOBs	17	519
Operating frequency	350 Mhz	
Power	120 mW	

5. Conclusion

A design and implementation of FM demodulator, and receiver is presented. Simulations examines the performance of the design and it shows perfect operation. The proposed system is implemented using Xilinx Vitrex-7 XC7VX550t board consumes 120mW and operates with 350 MHz

Funding: "This research received no external funding"

Conflicts of Interest: "The authors declare no conflict of interest."

References

[1] B. Sklar, F. Harris, Digital Communications: Fundamentals and Applications, 3rd edition, Pearson, 2020.
[2] Fuyun Ling, Synchronization in Digital Communication Systems 1st Edition, Cambridge university press, 2017.
[3] V. Bagad, Wireless Communication. Technical Publications, 2009.
[4] Thomas Paul Weldon, Analog and Digital Communication Lecture Notes,
[5] B. lathi, Z. Ding, Modern Digital and Analog Communication, 5th edition, Oxford university press, 2018.
[6] H. Xiao, X. Liu and L. Zhou, Design of PCM/FM Baseband Modulation Transmitter Based on Software Radio, 2018 Eighth International Conference on Instrumentation & Measurement, Computer, Communication and Control (IMCCC), 714-717, 2018.
[7] X. Huang, Research on variable rate PCM/FM telemetry modulation and demodulation technology, 2016 IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB), 1-5, 2016.

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

[8] Z. Wan, W. Rhee and Z. Wang, "A Nonlinearity-Calibration-Free Reconfigurable ADPLL for General Purpose Frequency Modulation," 2020 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), 19-20, 2020.
[9] S. Wenyou and H. Yonghong, "Design and Realization of Direct PLL FM Transmitter for UAV Data Link," 2009 WASE International Conference on Information Engineering, 522-525, 2099.
[10] S. J. A. Bakar, S. Setumin and A. I. C. Ani, "PLL System with Active PI Filter for FM Demodulation Application," 2022 IEEE 13th Control and System Graduate Research Colloquium (ICSGRC),151-154, 2022.
[11] B. Schlecker, M. Dukic, B. Erickson, M. Ortmanns, G. Fantner and J. Anders, Single-Cycle-PLL Detection for Real-Time FM-AFM Applications, in IEEE Transactions on Biomedical Circuits and Systems, vol. 8(2), 206-215, 2014.
[12] J. Lee, Y. Baek, I. Eo and B. Koo, A Ka-Band FMCW PLL Synthesizer with 8.5-GHz Bandwidth for High-Precision High-Resolution Sub-mmWave Radar Sensing, 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5, 2021.
[13] Salamai, Abdullah Ali, El-Sayed M. El-kenawy, and Ibrahim Abdelhameed. "Dynamic voting classifier for risk identification in supply chain 4.0." CMC-COMPUTERS MATERIALS & CONTINUA 69, no. 3 (2021): 3749-3766.
[14] Forouhar Farzaneh; Ali Fotowat; Mahmoud Kamarei; Ali Nikoofard; Mohammad Elmi, 3 PLL, FM Modulation, and FM Demodulation, in Introduction to Wireless Communication Circuits, River Publishers, 125-168, 2020.
[15] A. S. Prabhu and V. Elakya, Design of modified low power booth multiplier, 2012 International Conference on Computing, Communication and Applications, 1-6, 2012.
[16] D. Govekar and A. Amonkar, Design and implementation of high speed modified booth multiplier using hybrid adder, 2017 International Conference on Computing Methodologies and Communication (ICCMC), 138-143, 2017.
[17] Eid, Marwa M., El-Sayed M. El-kenawy, and Abdelhameed Ibrahim. "A binary sine cosine-modified whale optimization algorithm for feature selection." In 2021 National Computing Colleges Conference (NCCC), pp. 1-6. IEEE, 2021.
[18] D. Kalaiyarasi and M. Saraswathi, Design of an Efficient High Speed Radix-4 Booth Multiplier for both Signed and Unsigned Numbers, 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), 1-6, 2018.
[19] G. P. Ao, The Basic Principle and FPGA Implementation of NCO, 2012 Second International Conference on Instrumentation, Measurement, Computer, Communication and Control, 90-94, 2012.
[20] El-kenawy, El-Sayed M., Hattan F. Abutarboush, Ali Wagdy Mohamed, and Abdelhameed Ibrahim. "Advance artificial intelligence technique for designing double T-shaped monopole antenna." CMC-COMPUTERS MATERIALS & CONTINUA 69, no. 3 (2021): 2983-2995.
[21] S. Hu, H. Li and J. Huang, An Optimal Algorithm for Designing NCO Circuit in Mobile Communication Systems," 2009 WRI International Conference on Communications and Mobile Computing, 372-376, 2009.
[22] L. Zhihua and W. Weilian, "The design of NCO based on CORDIC algorithm and implementation in FPGA(∗)," 2011 International Conference on Electronics, Communications and Control (ICECC), 2902-2905, 2011.
[23] M. Asif and Z. Ahmed, "Design of Optimized NCO for FSK Modem," 2005 Student Conference on Engineering Sciences and Technology, 1-4, 2005.
[24] M. Saber, Y. Jitsumatsu, Y. M.T.A. Khan, A Simple Design to Mitigate Problems of Conventional Digital Phase Locked Loop, Signal Processing: An international journal (SPIJ), vol.6 (2),65-77, 2012.
[25] J. Guojun and S. Wenzhong, "Stability of bilinear time-delay systems," in IMA Journal of Mathematical Control and Information, vol. 18(1) 53-60, 2001.
[26] Zhang Tingting et al., "An s-z domain transformation method for the readout circuit design of closed-loop micromechanical capacitive accelerometer," 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC), 1-3, 2012.
[27] M. Saber and Y. Jitsumatsu and M. T. A. Khan, Low Noise-Low Power Digital Phase-Locked Loop, IEEE Region 10 Conference (TENCON) 2010, 1324-1329, Nov. 2010.
[28] M. Saber, Y. Jitsumatsu and M. T. A. Khan, Design and Implementation of Low Power Digital Phase - Locked Loop, in Proc. of 2010 Int. Sympo. on Spread Spectrum Techniques and Applications, 928-933, 2010.
[29] Mohamed Saber, Efficient Phase Recovery System, Indonesian Journal of Electrical Engineering and Computer Science, vol.5 (1), 123-129, 2017.
[30] Mohamed Saber, A novel design and Implementation of FBMC transceiver for low power applications, Indonesian Journal of Electrical Engineering and Informatics, vol. 8(1), 83-93, 2020.

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022

[31] R. Das, A. Guha and A. Bhattacharya, "FPGA based higher order FIR filter using XILINX system generator," 2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), 111-115, 2016.
[32] Z. J. Xiang, L. Wang, Y. Jiang, D. Liu and J. Wang, "A Framework for Xilinx SRAM-based FPGA Functional Test," 2020 IEEE 3rd International Conference on Electronics and Communication Engineering (ICECE), 207-210, 2020.
[33] P. Priya and S. Ashok, "IIR Digital Filter Design Using Xilinx System Generator for FPGA Implementation," 2018 International Conference on Communication and Signal Processing (ICCSP), 0054-0057, 2018.

DOI: https://doi.org/10.54216/IJWAC.040206
Received: January 03, 2022 Accepted: May 22 2022