Photonic Crystal Circuitry and its Impact on Wireless Networks

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Abstract

Wireless networks are considered a hot topic in dealing with data without need to routers or other infrastructures. Each node has a part of routing responsibility. This result to a huge of data in forwarding to other nodes and will need high speed to process. Photonic crystal applications come to solve the necessity for such speed with small circuitry area. One of the main factors that affect their operation is the structure topology. Ring resonator, cavity based structures, self-collimation, and waveguide approaches are some of these topologies. OR gate is proposed in this paper to be simulated and evaluated as one of the basic element block. This design is built on a square lattice-photonic crystal construction on a ring resonator basis. Rotation of 90, 180, and 270 degrees are applied in clockwise direction. Sensitivity analysis, and carefully rod locations are considered to obtain remarkable performance. Minimum size and highly data rate are two characteristics that discriminates this design. The minimum size of 51.48 μm^2 is obtained. The bit rates of 1.35, 6.35, 3.2, and 2.53 Tb/s are calculated with the 0, 90, 180, and 270 degrees, respectively. Comparison table is well organized for the recently published photonic crystal OR-gate that based on ring resonator. Finite difference time domain and Plan wave expansion method are used to analyze the proposed structure at 1.55μm wavelength to verify OR- gate operation.

Keywords: Wireless networks; OR-gate; Photonic crystal applications; Ring resonator; Photonic crystal topology; Bit rate.

1. Introduction

Miniaturization of the circuit size, high speed data processing, and digital computing are the main direction for new technologies such as wireless network. Different electronic circuits are fabricated based on semiconductor materials [1, 2]. Logic designs that classified as combinational and sequential are fabricated to perform different operations [3]. The high necessity for high data rate; let the electronic devices reach to their bottle nick. Optical circuit models were proposed to implement high-speed applications with a small area. Semiconductor optical amplifiers (SOA) [4], periodically poled lithium niobate (PPLN) waveguides [5], and photonic crystal (Ph. Cs.) [6] are some forms inherent to the optical world.

The advantages of light speed contribute the (Ph. Cs.)-technology to provide high speed applications like sensors [7], filters [8], logic gates (i.e., AND, OR, XOR) [9], multiplexers [10], demultiplexers

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[11], flip-flops [12], encoders [13], decoders [14] and half adders [15]. (Ph. Cs.) can be defined as artificial crystals that have highly ordered dielectric materials which lowering consumption of the waste power [6].

Several applications can be formed when changing the basic structures topology. These topologies can be classified into ring resonator, self-collimation, waveguide, and cavity. Recently published paper that dealing with the different characteristics between them was discussed in [16]. Square and hexagonal shape lattice types were shown in literature [17, 18]. The operation could be done in linear and nonlinear regime. RSOFT [19] (i.e., its numerical technique is finite difference time domain (FDTD)) and COMSOL [20] (i.e., mainly operate on finite element method (FEM)) are two software packages that are used to simulate and analyse (Ph. Cs.) structures.

In this article, two dimensional (Ph. Cs.) OR gate ring resonator based are carefully examined and verified. The figures of merits such as: contrast ratio (CR), the size of the structure, bit rate (BR), and linearity will be represented.

This paper is organized as follows. Section 2 covers the structure details. Simulations and results can be found in sections 3. The conclusions are presented in section 4 followed by the most relevant references.

2. Structure details

A. Basic Concepts

The OR- gate is considered one of the digital logic block elements. It can be shown as two inputs and one output. Its output goes high when at least one its inputs are high. However, the output goes low when all inputs are low. The Boolean expression and the related truth table are defined in equation (1) and table 1, respectively [3]:

$$Q=A+B \qquad (1)$$

Table 1: OR- gate truth table

Input		Output
A	*B*	*OR*
0	0	0
0	1	1
1	0	1
1	1	1

B. Basic Concepts

The proposed structure is built on a two-dimensional (Ph. Cs.) square lattice with a lattice constant (a) (i.e., the distance between the center of two rods) of 0.6 µm. It consists of (11X13) Silicon (Si) rods in air substrate. The rod radius (r) = 0.12 µm and has the material with refractive index (n) = 3.4. The design consists of two inputs and one output as shown in Fig. 1. The ring resonator is the core element in the proposed design that will be rotated to examine its effect on this design. One waveguide is used to guide the lunched light from input (*A*). The position of the output ports is selected by applying sensitivity analysis. This location provides the best performance and output power response in comparison to the shifted versions of the output ports.

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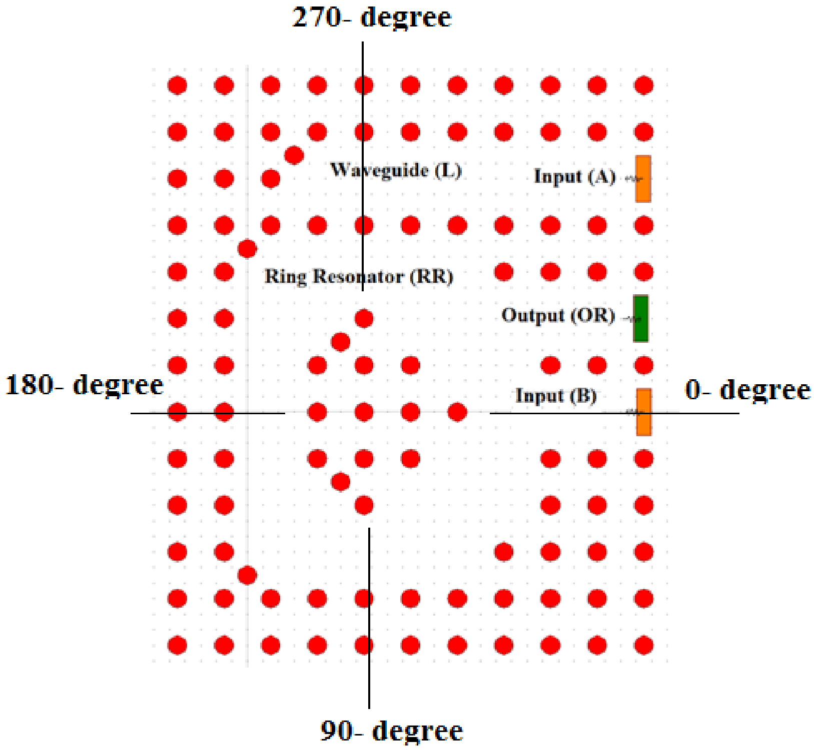

Figure 1: the proposed photonic crystal OR- gate structure with no rotation

3. Simulation of the Proposed Gate

A. Numerical Methods and Photonic Band Gap (PBG) Range

Finite-difference time domain (FDTD) is one of the numerical methods that are used to simulate (Ph. Cs.) structures. The power distribution, the time response, and the power level for each state are introduced. The photonic band gap (PBG) (i.e., the forbidden optical range that light cannot propagate) is calculated by using plane wave expansion (PWE) method. The designs are simulated by applying transverse electric (TE) field.

From Fig. 2, the (PBG) range is between 1.395 μm and 2.143 μm. The position of input ports and output port is located as shown in Fig. 1 by using sensitivity analysis. Ring resonator topology is carefully designed to operate in the C-band optical wavelength (i.e., between 1530 to 1565 nm).

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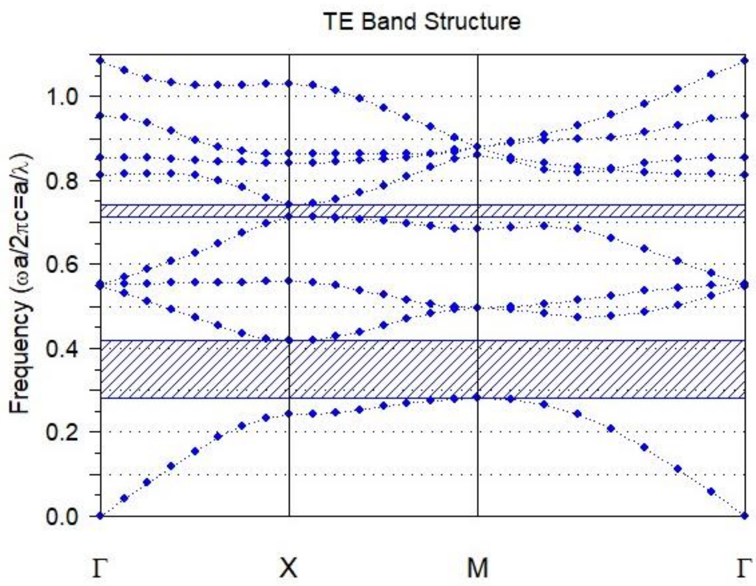

Figure 2: the photonic band gap (PBG) of TE- polarization

B. The Proposed OR Gate Operation

In this section, the power distribution and the time response are investigated. The results are executed at 1.55 μm wavelength. Four states will be explained in the following section to verify the operation and to extract the valued results. The output power levels are normalized. As shown in Fig.1, the output will be switched on and off based on the state of the two inputs as will be shown.

1) Case 1: when no power is applied to both inputs, there is no power at the output port.

2) Case 2: when one of the inputs is on (i.e., input A=1, B=0) a light wave will propagate through the waveguide and mutually couple into ring resonator. The power that exists now in the ring resonator is guided with the effect of the scattering rods to arrive to the output. Figure 3, displays this state with output equals 0.6 and which is considered logic (1).

3) Case 3: on the other hand, when the input power lunched through port B (i.e., B=1) and the other port is disabled (i.e., A=0). The applied signal is circulated within the ring at its resonant wavelength (i.e., 1.55 μm) to deliver the power directly to the output port. The output is logic (1) with the power level of 0.98 as shown in Fig. 4.

4) Case 4: when both inputs (i.e., A and B) are logic (1). Figure 5 demonstrates a constructed field is done between the two input beams. The result of this case is to confirm OR-gate operation as the output is equal 0.75.

When a rotation of the inner ring resonator is applied by 90, 180, and 270 degrees are applied; new records are obtained. Figures 6 discriminates the new position for each rotation. The accompanying results are represented in Fig. 7 to Fig. 15. Table 2 displays the power levels and the calculated bit rates at each position. Unfortunately, that any rotation with another angles such as 45, 135, and 225 degrees not verify the OR- gate operation and gives bad results.

C. Bit Rate (BR) calculation

The bit rate is defined as the reciprocal of the response time (RT) as show in equation (2) [9].

$$RT = t_d + t_r + t_f = t_d + 2t_r \qquad (2)$$

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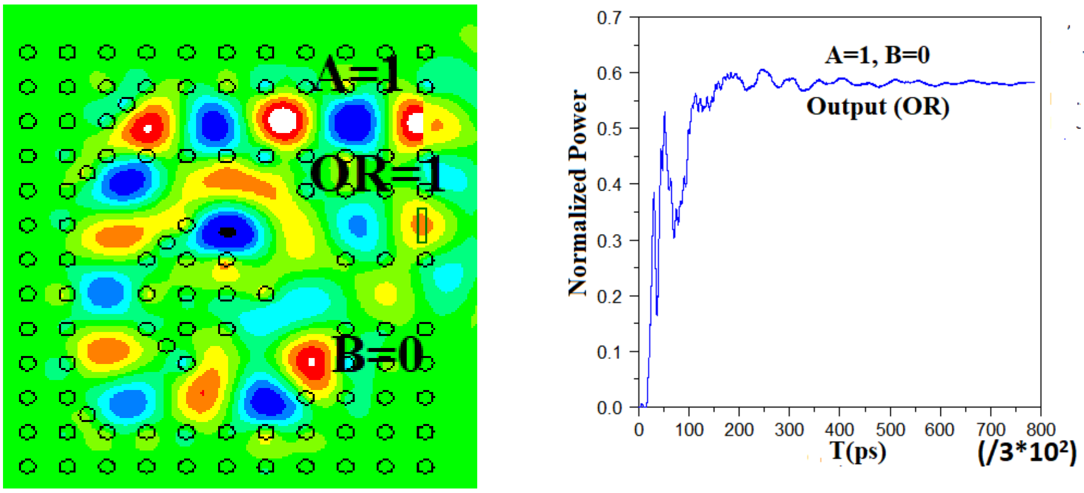

Figure 3: A = 1 and B = 0 (a) power distribution, (b) time response

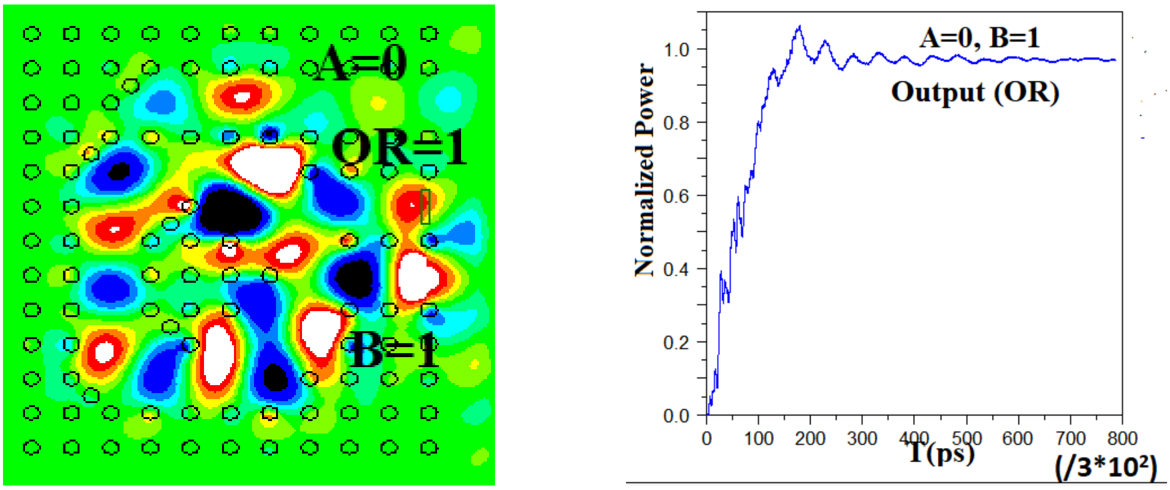

Figure 4: A = 0 and B = 1 (a) power distribution, (b) time response

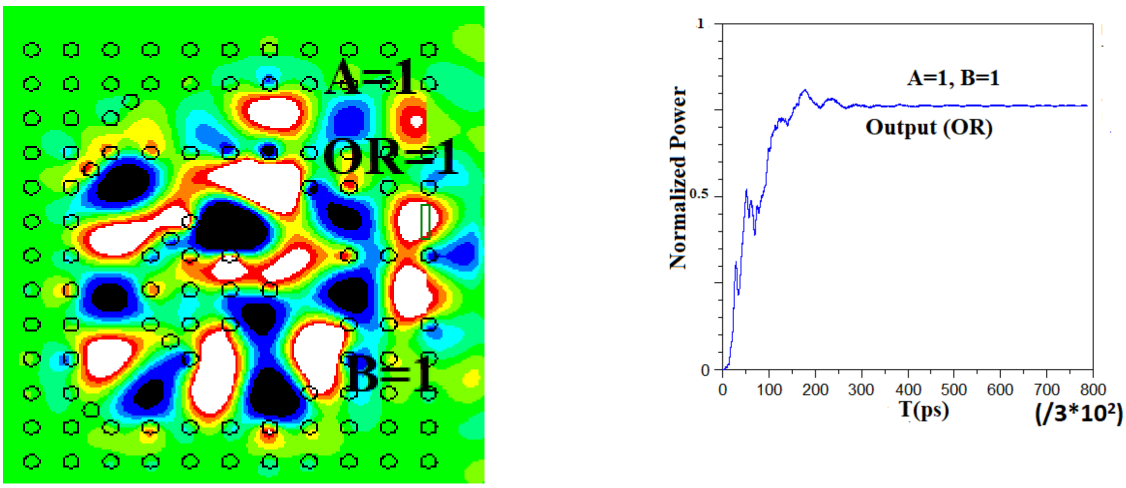

Figure 5: A = 1 and B = 1 (a) power distribution, (b) time response

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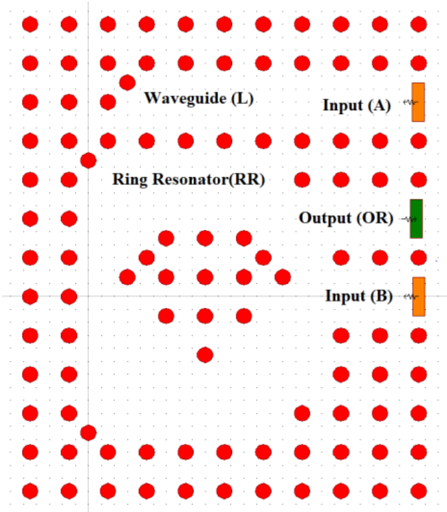
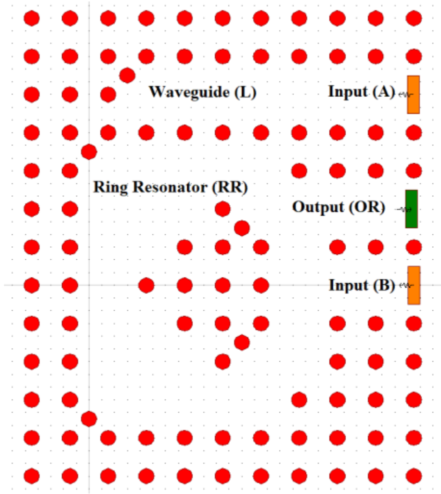
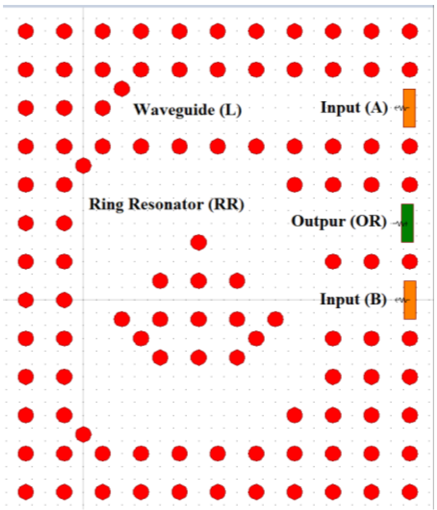


(a)



(b)



(c)

Figure 6: the proposed structure with rotation (a) 90- degree, (b) 180- degree, and (c) 270- degree

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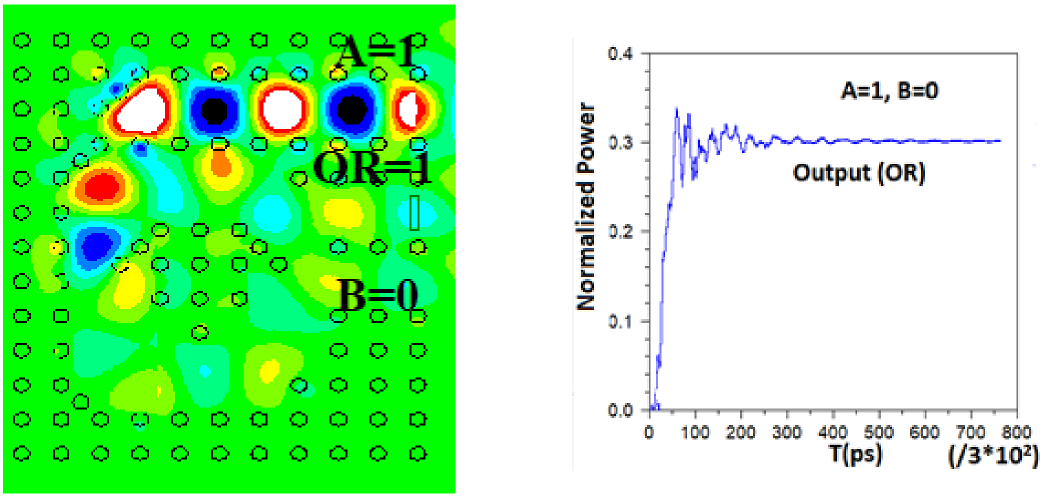

Figure 7: A = 1 and B = 0 (a) power distribution, (b) time response for 90-degree rotation

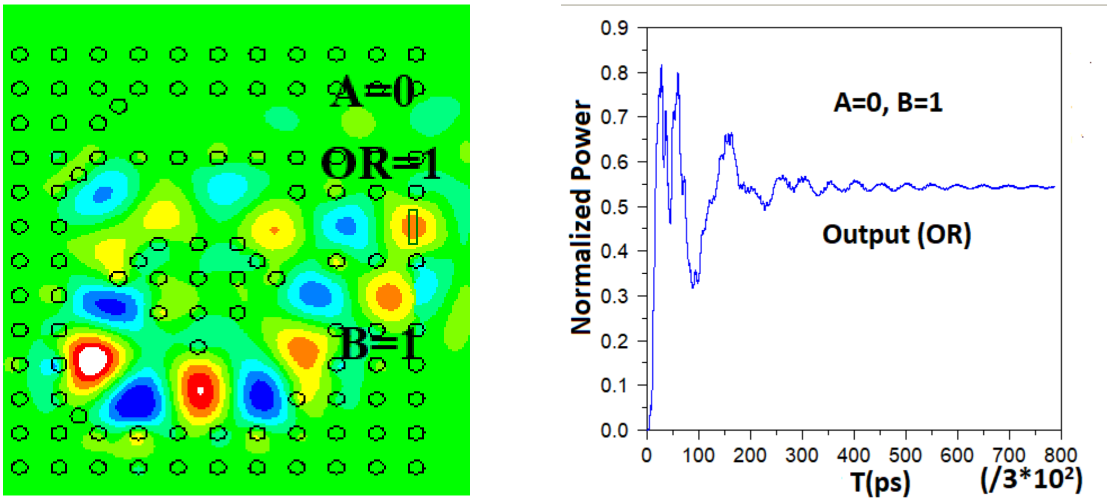

Figure 8: A = 0 and B = 1 (a) power distribution, (b) time response for 90-degree rotation

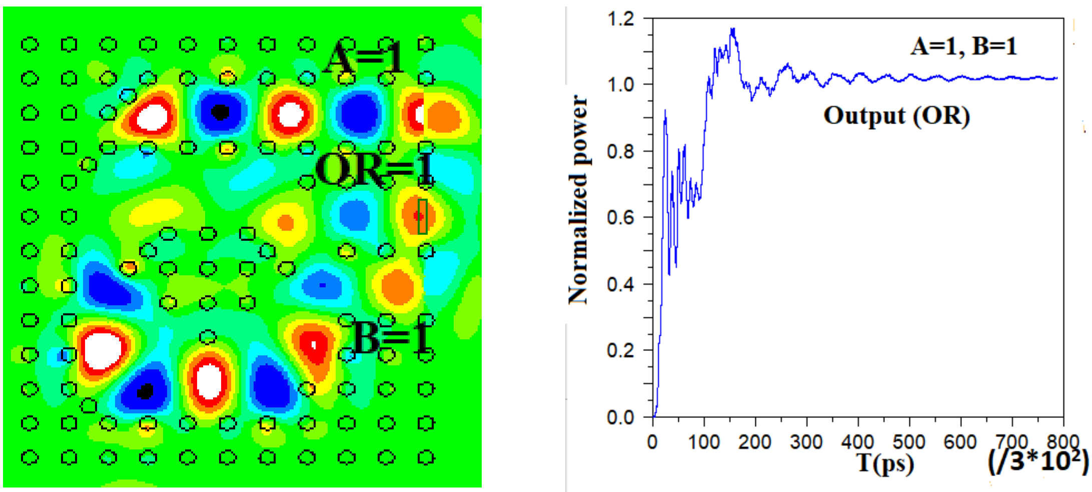

Figure 9: A = 1 and B = 1 (a) power distribution, (b) time response for 90-degree rotation

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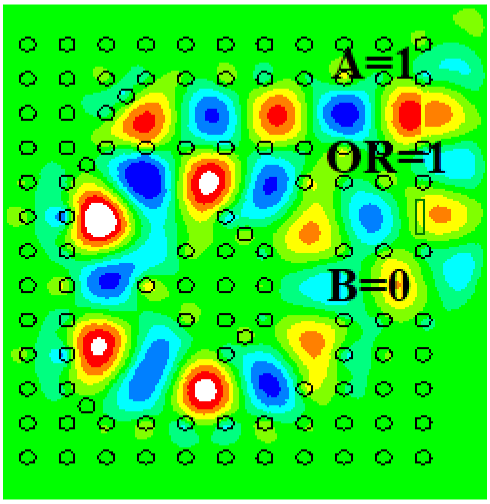
Where the delay time (t_d) is the time taken to go up the output power from 0 to 10% of the steady-state output power. The time that is taken between 10% to 90% of the average output power is called transition time (t_r). The falling time (t_f) is the time for final steady-state power to 10%, which is approximately equal to (t_r) in linear material scenarios as in [9]. The (BR) is calculated from the time response to be 1.35 Tp/s.



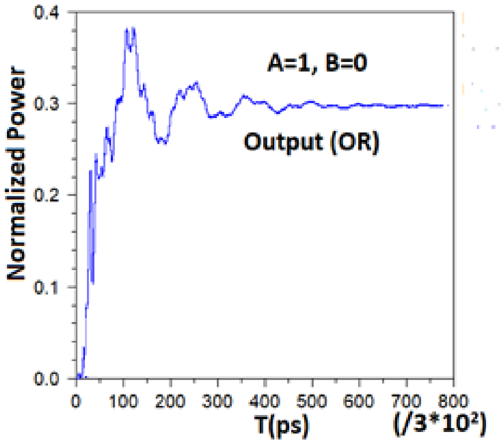
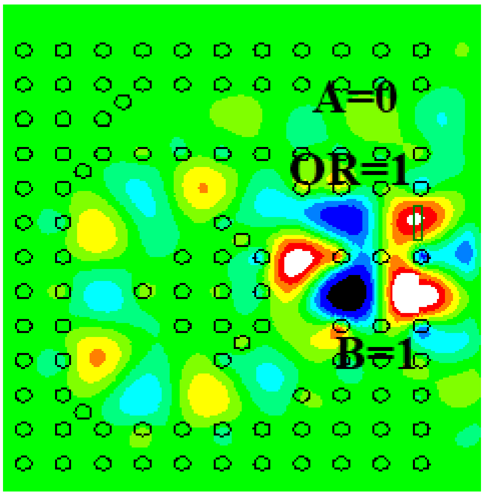


Figure 10: A = 1 and B = 0 (a) power distribution, (b) time response for 180-degree rotation



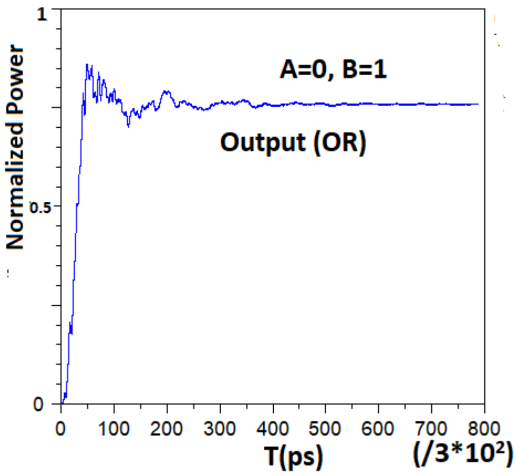


Figure 11: A = 0 and B = 1 (a) power distribution, (b) time response for 180-degree rotation

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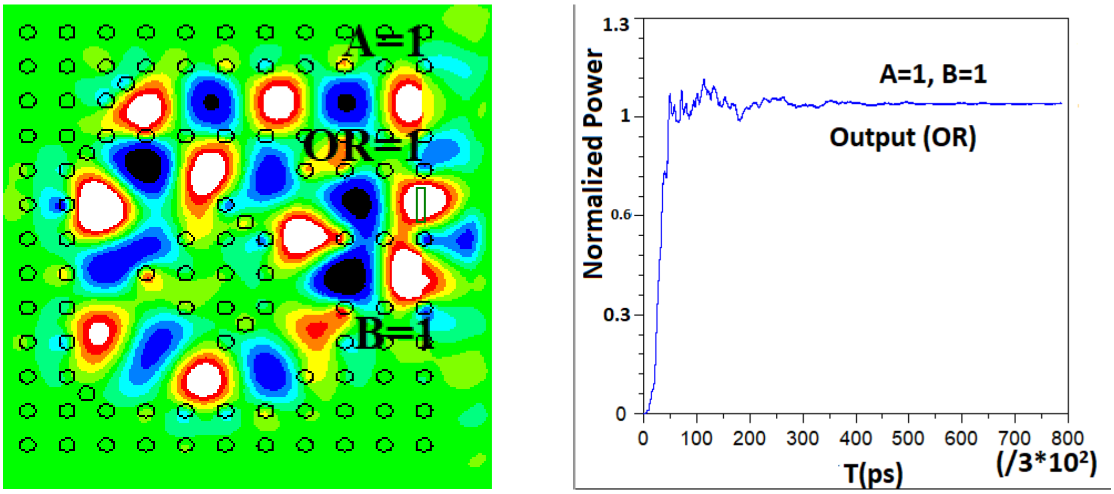

Figure 12: A = 1 and B = 1 (a) power distribution, (b) time response for 180-degree rotation

As will be shown, table 3 includes the analogy between the proposed structure and its counterpart in the literature. Most of the designs are used (Si) as the rod material. The maximum number of gates appears in [27]. The maximum size with 1287 μm^2 exists in [30]. The highest (CR) occur in [31] in a hexagonal shape lattice type with only OR- gate as in table 3. The intended structure for the OR-gate has minimum size and the high (BR) with ring resonator rotation of 90-degrees. It can be implemented with the same rod radius. No need for any auxiliary inputs to verify the operation.

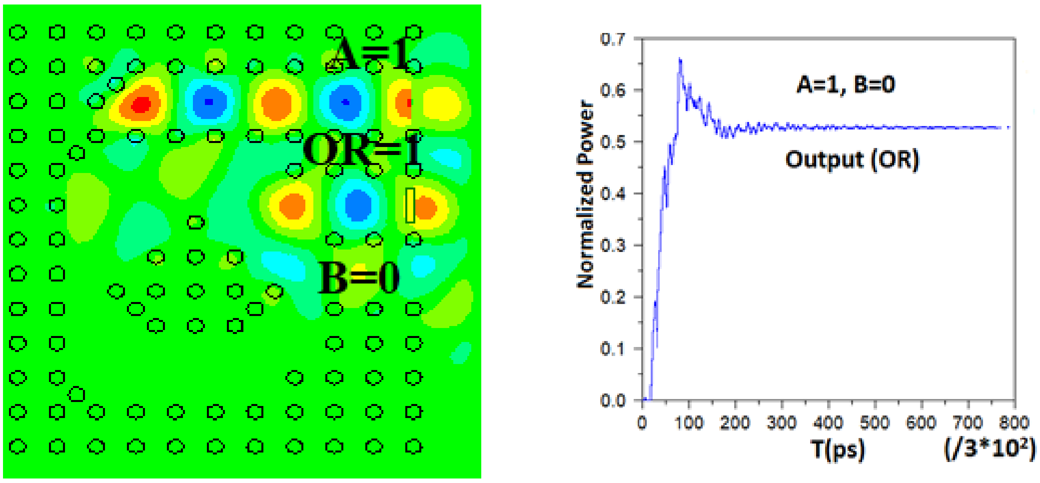

Figure 13: A = 1 and B = 0 (a) power distribution, (b) time response for 270-degree rotation

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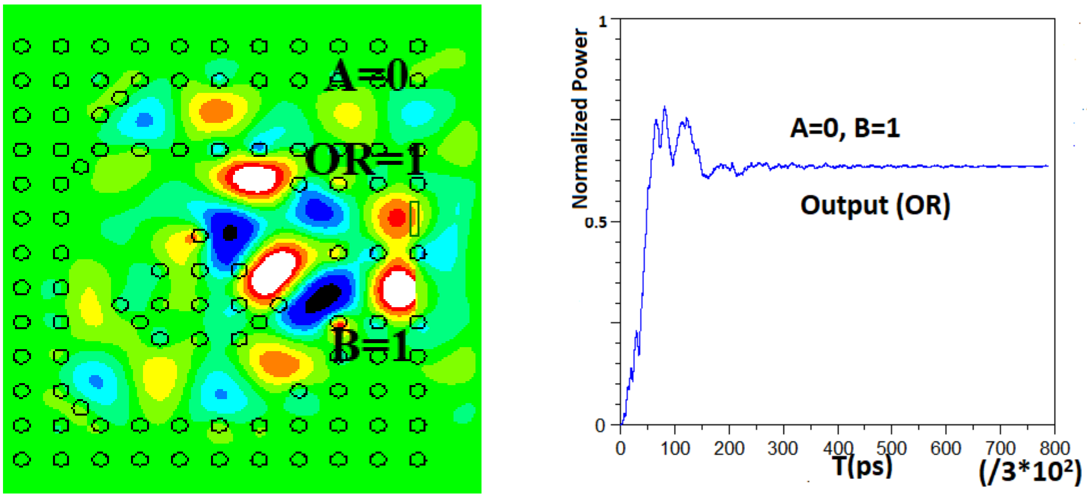

Figure 14: A = 0 and B = 1 (a) power distribution, (b) time response for 270-degree rotation

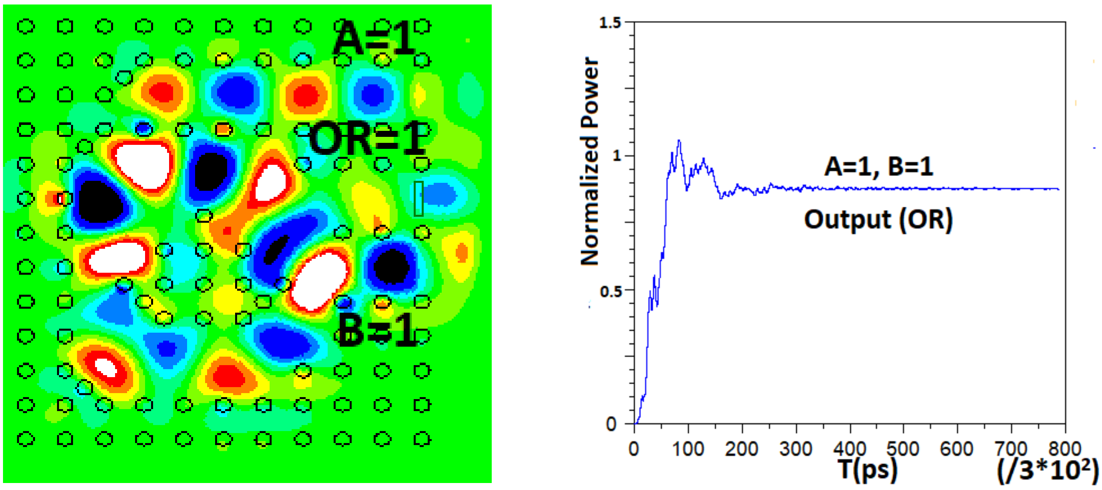

Figure 15: A = 1 and B = 1 (a) power distribution, (b) time response for 270-degree rotation

Table 2: the power levels and the calculated bit rate for each rotation angle

Input		0- degree		90- degree		180- degree		270- degree	
A	B	power	(BR) Tb/s	power	(BR) Tb/s	power	(BR) Tb/s	power	(BR) Tb/s
0	0	0	1.35	0	6.35	0	3.2	0	2.53
0	1	0.98		0.55		0.75		0.6	
1	0	0.6		0.3		0.3		0.56	
1	1	0.75		1		1.0		0.8	

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Table 3: comparison between the published all- optical OR- gate ring resonator based in the literature

Ref. and Year	Contrast ratio (dB)	Bit rate (Tb/s)	Size (μm^2)	Auxiliary input	Implemented gates
Ref [21-2015]	16.7	0.33	136	√	OR, AND, XOR
Ref [22-2015]	4.77	0.2	303	√	OR, AND, XOR , NOT
Ref [23-2015]	18.7	0.33	499	√	OR, NOT
Ref [24-2016]	NA	0.8	200	X	OR
Ref [25-2017]	NA	0.33	134	X	OR, AND
Ref [26-2017]	25	0.13	283	√	OR , NOR
Ref [27-2017]	NA	3.8	132	X	OR, AND, XOR, NOT, NOR, NAND, XNOR
Ref [28-2018]	9.29	NA	335	√	OR, AND, NAND
Ref [29-2019]	18	4.7	250	√	OR,AND
Ref [30-2019]	19	0.5	1287	√	OR
Ref [31-2021]	29	5	454	√	OR
Ref [32-2022]	NA	2.5	56.2	X	OR
Ref [33-2022]	NA	5.02	56.16	X	OR, XOR, NOT
Proposed (0-degree)	NA	1.35	51.48	X	OR
Proposed (90-degree)	NA	6.35	51.48	X	OR
Proposed (180-degree)	NA	3.2	51.48	X	OR
Proposed (270-degree)	NA	2.53	51.48	X	OR

4. Conclusion

The OR gate with new proposed design is implemented in this paper. It can be used as a basic element block for other circuits to be used in a wireless networking. A rotating ring resonator is used to implement OR-gate with rotating angles of 90, 180, and 270 degrees in clockwise direction. The performance and the figures of merits are calculated. This design operates in linear regime that let them to save the power consumption. FDTD and PWE methods are the two numerical techniques that are used for simulation and analysis. The core for this module is the ring resonator topology. Therefore, the comparison table is organized and concentrates on the same logic with this topology type. The main targets are to verify OR logic gate and to get the minimum size and high bit rate with respect to the other published papers in literature. The future work is to implement and build more complex circuits that characterized by their speed and minimum size.

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