A PSPICE Fast Model for the Single Electron Transistor

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Abstract

Motivated by the merits of low power dissipation, ultra small size, and high speed of many nanoelectronic devices, They have been demonstrated to ensure future progress. Single electron devices became one of the most important nanoelectronic devices due to their interesting electrical characteristics and behavior. Many research efforts moved to describe their electrical characteristics to use them with conventional electronic devices. This paper deals with modeling and simulation of such new electronic devices. This paper presents a model for the Single Electron Transistor (SET) and its application in simulating hybrid SET/MOS ADC and DAC converters. This model uses the orthodox theory of single-electron tunneling and determines the average current through the transistor. The proposed model is more flexible that is valid for large range of drain to source voltage, valid for single or multi gate SET and symmetric or asymmetric SET. Finally, using this model with MOSFET transistors to realize a multi-bit Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). The hybrid n-bit DAC nano-circuits are simulated for (n=4 and 8) using Orcad Capture PSPICE. The performance of the SET/MOS hybrid n-bit ADC circuits were simulated (for n=3 and 8). The results show that the transient operation of hybrid SET/MOS circuit-based DAC could successfully operate at 1000K while ADC could operate at 144K. This performance can be compared with the pure SET circuits, the proposed converter circuits have been enhanced in the drive capability and the power dissipation. Compared with the oth`er SET/MOS hybrid circuit, the implemented converter circuits have low simulation time, high speed, high load drivability and low power dissipation.

Keywords: Single-Electron Transistor (SET), MOS transistor; Nano-circuits, hybrid; simulation, orthodox theory, PSPICE; Master Equation, Tunnel Junction (TJ), Coulomb blockade

1. Introduction

The size miniaturization in microelectronic circuits has been an important factor to the emotional increment in the processing power of computer arithmetic circuits. However, it is generally accepted that sooner or later MOS based circuits cannot be reduced further in feature size due to fundamental physical restrictions [1].

The fast progress in the fabrication technology of silicon nano devices has pushed the device dimensions toward nanometer scale. When device dimensions are reduced to a few nanometer range, the single electron tunneling leads to interesting new device characteristics. If we wished to continue obeying the Moore law and make the circuits cheaper, faster and the power dissipation lower, some new electronic devices would have to be created, such as Single-Electron Transistor (SET) [2].

Single Electron Transistor (SET) is expected to be the future of VLSI design due to its nanoscale feature-size, ultra low power dissipation and high density. The fundamental principle of single-electronic is the Coulomb blockade, which was first observed and studied by Gorter [3]. Pure SET circuits have very limited applications due to SET's low current drivability, small voltage gain and low-temperature operation.

Since MOS devices have advantages that can compensate for the disadvantages of SET, hybrid SET/MOS architecture which combines the advantages of both MOS and SET. The basic single-electron nano-devices is the tunnel junction which can be thought of as a leaky capacitor. The SET consists of two tunnel junctions in series

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sharing a common electrode, which is called the island, also known as the quantum dot and two gates are coupled to the island.

The orthodox theory describe the transportation of charge using free energy, tunnel rates, coulomb blockade and quantization of charge. Most single electron transistor models are based on the orthodox theory. Some models depend on the tunneling of an electron through a barrier. Once the tunneling rates for all junctions are known, the tunneling probabilities and tunneling current are calculated. Thus the single electron systems can be simulated.

Analog and digital converters are important circuits. The Analog-to-Digital Conversion (ADC) and Digital-to-Analog conversion (DAC) are developed to obtain high integration density, high speed, and low power dissipation. The advantages of ADC and DAC circuits which uses the Single Electron Transistor are low power dissipation, high integration density and high speed. Some research groups had proposed several kinds of ADC and DAC circuits based on SET [4]–[9].

A proposed hybrid SET/MOS DAC and ADC circuits were presented in this paper to take the advantages of the SET and the MOS. Their advantages are low power dissipation, small size and high load capability.

In this paper, we proposed a model for the SET. This model is based on the “orthodox theory” of single electron tunneling. It is valid for unlimited range of drain to source voltage, valid for single or multi gate SET and symmetric or asymmetric SET. SET characteristics produced by the proposed model have been verified against Monte Carlo simulator SIMON[10] and show good agreement. This model is computationally efficient in comparison with the existing models. The ADC and DAC circuits are simulated using the proposed PSPICE model and MOS transistors.

Moreover, This paper deals with modeling and simulation of such new electronic devices It starts with describing single electron phenomena and discussing the most important theory orthodox theory of single electronics used in explanation of single electron devices behavior With the aid of orthodox theory and the basic idea of electron transport through tunnel junctions it presents an equivalent circuit model for Single Electron Transistor SET taking into consideration the effect of temperature tunneling resistance and gate capacitance The proposed model is validated by comparing its results with well recent known models The model is tested using a popular single electron simulator named SIMON This chapter also presents a study about different modeling techniques Master equation and Macromodeling algorithm for single electron systems These techniques could model the most used single electron device single electron transistor SET By applying these techniques one can find that master equation gives better accuracy than Monte Carlo algorithm and takes less simulation time A proposed PSPICE fast model for the SET is presented It is based on the “orthodox theory” of single electron tunneling valid for unlimited range of drain to source voltage valid for single or multi gate SET and symmetric or asymmetric SET It is implemented using PSPICE to enable simulation with other electronic components like MOS devices Some single electron circuits are studied and simulated using our proposed model These circuits are single electron inverter five inverters in series and amplifier circuit Finally this chapter presents a design and simulation of hybrid SET/MOS Analog to Digital and Digital to Analog circuits The hybrid n bit DAC nano circuits are simulated for n=4 and 8 using Orcad PSPICE The performance of the SET/MOS hybrid n bit ADC circuits were simulated for n=3 and 8 Also ADC circuits using Single Electron Transistor were simulated for n=8 using Orcad PSPICE The results show that the transient operation of hybrid SET/MOS circuit based DAC could successfully operate at 1000K while ADC could operate at 144K This performance can be compared with the pure SET circuits the proposed converter circuits have been enhanced in the drive capability and the power dissipation Compared with the other SET/MOS hybrid circuit the implemented converter circuits have low simulation time high speed high load drivability and low power dissipation

The proposed SET model is presented in section 2. The proposed model implementation is illustrated in section 3. Section 4 describes the comparison between the proposed model and other models. DAC using hybrid SET/MOS circuit is illustrated in section 5. ADC using hybrid SET/MOS circuit is introduced in section 6. Finally, conclusions are given in section 7 followed by the references.

2. The proposed set pspice model

Figure 1 shows the Single Electron Transistor symbol with one gate connection (three terminal). Our circuit simulation model, solves the steady state master equation taking into consideration the effect of the tunneling resistance and temperature variations. Fig. 2 shows a complete circuit simulation model for the SET. It consists of two tunnel junctions, each is modeled by a capacitance connected in parallel to a resistance, a gate is coupled to the island. A voltage source is connected to the source, the drain, and the gate.

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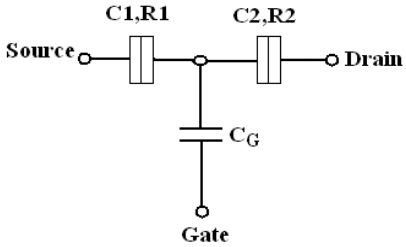

Fig. 1: Single Electron Transistor symbol

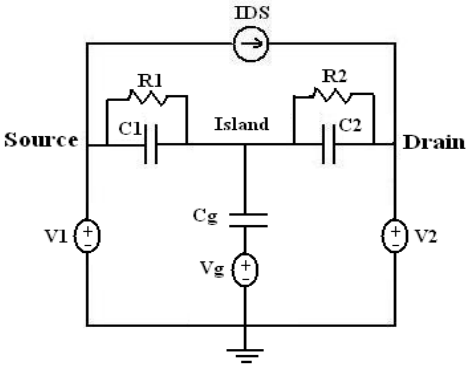

Fig. 2: Single Electron Transistor model in PSPICE

This model is for a one gate connection (three leg) transistor with zero gate current and with drain source current depending on the drain, source and gate voltages. The model is based on mathematical relation based on the orthodox theory. The code is structured in four sections, section 1 is the device parameters, section 2 is the general functions, and section 3 is the recursion relation, while the last section is for current calculations. The code used in PSPICE model editor sub-circuit presents a three nodes device; terminals 1 and 2 as the drain and source, 3 is the gate terminal. The code for the parameter and function equations involving the number of electrons in the island and the tunnel rate. Our model is developed on the following assumptions:

[1] 1. It obeys the orthodox theory of single electron tunneling.
[2] 2. The interconnect capacitances associated with the gate, source, and drain terminals are much larger than the device capacitances.

The voltage of the island when a charge *ne* is present on the island is:

$$V(n) = \frac{(ne + C_1V_1 + C_2V_2 + C_gV_g)}{C_\Sigma} \quad (1)$$

Where *e* is the positive elementary charge, *n* is an integer that specifies the number of elementary charges that have been added in the island, and C_Σ is the total capacitance:

$$C_\Sigma = C_1 + C_2 + C_g \quad (2)$$

The change in energy ΔE when a charge e tunnels from a lead at voltage Vi to the island is:

$$\Delta E_i = -eV_i + eV(n) + e^2/(2C_\Sigma) \quad (3)$$

The junction tunnel rate, Γ_i, is formulated based on the orthodox theory and given by [12]:

$$\Gamma_i = \frac{\Delta E_i}{e^2 R_i (e^{\Delta E_i / k_B T} - 1)} \quad (4)$$

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Where R_i is the tunnel resistance, k_B is Boltzman's constant, and T is temperature in Kelvin.

The probabilities that the charge states are occupied can be determined from the recursion relation [12]:

$$P(n) = P(n-1)\left(\frac{\Gamma_{1R}(n-1)}{\Gamma_{2R}(n)+\Gamma_{1L}(n)}\right) \quad (5)$$

Where Γ_{iL}: is the tunnel rate which e can tunnel from left through tunnel junction i and Γ_{iR}: is the tunnel rate which e can tunnel from right through tunnel junction i.

The drain-source current is:

$$I = e\sum_{n=-\infty}^{n=\infty} P(n)(\Gamma_{1R}(n) - \Gamma_{1L}(n)) \quad (6)$$

3. Implementation of the proposed model

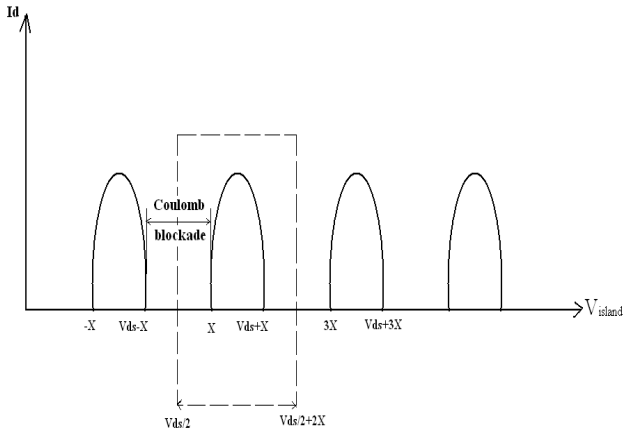
As shown in Figure 3, the drain to source current is a periodic function of V_{island} with periodicity of (2X). In this model, the drain to source current equation has been developed only for the period: $\frac{V_{ds}}{2} \le V_{island} \le 2X + \frac{V_{ds}}{2}$ (calculation zone which is shown in Figure 3. We can shift other values of V_{island} by an integral multiple of (2X) into this window and apply the same model to calculate the drain to source current.

As Vds range increases, the number of states that must be added into calculation also increases. The idea is to take only the dominant states, depending on the values of Vds.

We can determine which set of states are needed and also do that mathematically as follows:

$$V_{ds} = Ne/C_{\Sigma} \quad (9)$$

Where N is an even number.



[3]

[4] Fig. 3: Schematic of SET drain current (I_d) characteristics as a function of the island potential(V_i) at $V_{ds} \langle e/C_{\Sigma}$ and T=0K.

[5]

The set of states will be ((-N)/2):(N/2)). For example if $|V_{ds}| \le 4e/C_{\Sigma}$, the set of states will be (-2:2). Table 4.1 summarizes the set of states that are needed to capture different ranges of Vds.

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[6] Table 1: The set and number of states that are needed for different ranges of V_{ds}.

Range of V_{ds}	N (even no.)	Set of states $\left(\left(\frac{-N}{2}\right):\left(\frac{N}{2}\right)\right)$	Number of states
$2e/C_{\Sigma}$	2	(-1:1)=(-1,0,1)	3
$4e/C_{\Sigma}$	4	(-2:2)=(-2,-1,0,1,2)	5
$6e/C_{\Sigma}$	6	(-3:3)=(-3,-2,-1,0,1,2,3)	7
$8e/C_{\Sigma}$	8	(-4:4) =(-4,-3,-2,-1,0,1,2,3,4)	9
$10e/C_{\Sigma}$	10	(-5:5) =(-5,-4,-3,-2,-1,0,1,2,3,4,5)	11
$12e/C_{\Sigma}$	12	(-6:6) =(-6,-5,-4,-3,-2,-1,0,1,2,3,4,5,6)	13
$14e/C_{\Sigma}$	14	(-7:7) =(-7,-6,-5,-4,-3,-2,-1,0,1,2,3,4,5,6,7)	15

In order to validate our proposed PSPICE model, we compare the results with Recursion Relation Model (RRM) which was developed by Lientschnig et al. (Applied Sciences and DIMES, Delft University of Technology) [11]. As shown in Figure 5 the results of this model shows a good agreement with Recursion Relation Model (RRM) results and they give the PSPICE great flexibility to include isolated single electron transistors in hybrid SET-FET electronic circuits.

The proposed model has been verified against Monte Carlo simulator SIMON [10]. IDS-VGS characteristics are simulated using the proposed model for symmetric (R1=R2) and asymmetric (R1≠R2) SET as shown in Figure 6. Ids-Vds characteristics are also simulated for symmetric SET as shown in Figure 7. The effect of temperature on IDS-VGS characteristics of SET is shown in Figure 8.

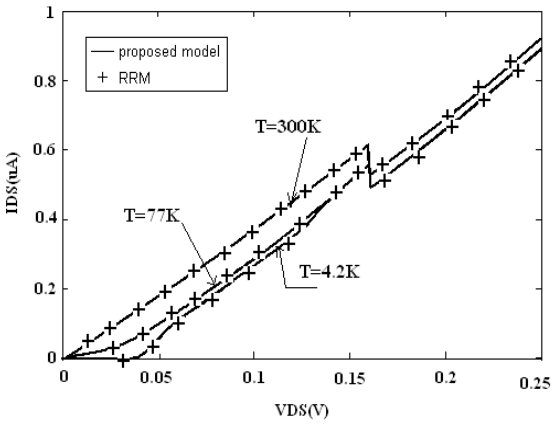

Fig. 5: Current-voltage characteristics (I_D-V_{DS}) of the proposed model and RRM model for T= 4.2K, 77K, 300K.

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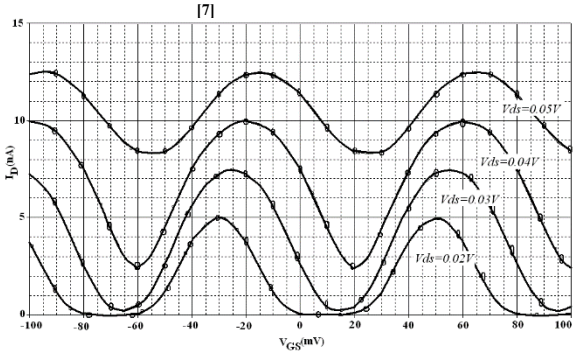
[7]



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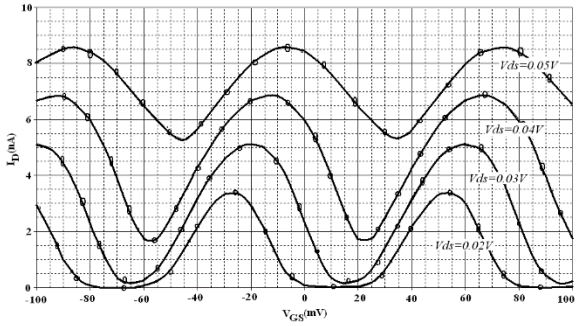

[9]

Fig. 6: Verification of the proposed model with device parameters, C_g=2aF, C_1=C_2=1aF, T=15K, V_{ds}=0.02-0.05 with step=0.01. (a) I_{DS}-V_{GS} characteristics for symmetric SET (R_1=R_2=1MΩ)

(b) I_{DS}-V_{GS} characteristics for asymmetric SET ((R_1=1MΩ, R_2=2MΩ)

The proposed model (lines), SIMON (symbols).

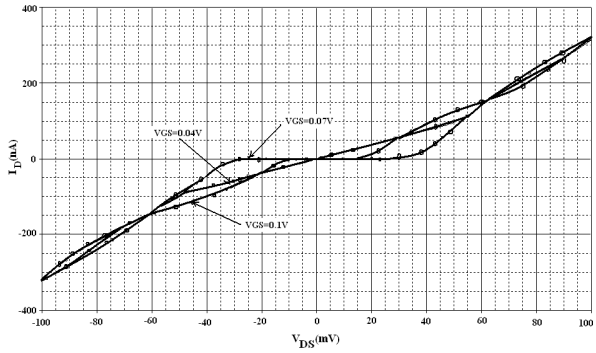

Fig. 7: I_{ds}-V_{ds} characteristics for symmetric SET with device parameters C_g=2 aF, C_1=C_2=1aF, T=15k, the proposed model (lines), SIMON (symbols).

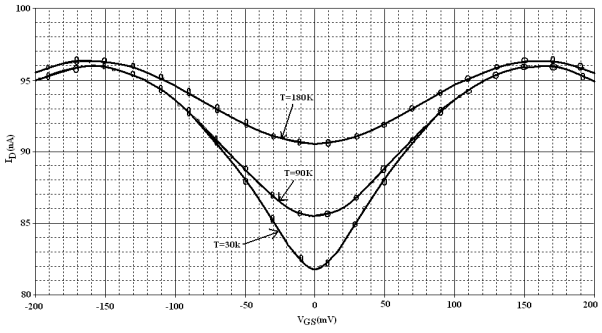

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Fig. 8: Effect of the temperature on SET characteristics with device parameters V_{ds}=0.32V,C_g=0.5aF, C_1=C_2=0.25aF, the proposed model (lines), SIMON (symbols).

4. Experimental results

Several research efforts on SET compact modeling have been reported, among of them: Lientschnig et al. [11] has introduced the recursion relation to solve the steady state master equation. It is valid for single or multi-gate and symmetric or asymmetric devices. It can capture V_{ds} range up to $5e/C_{\Sigma}$ using eleven states. However, using the proposed m/odel seven states are needed to capture drain to source voltage up to $6e/C_{\Sigma}$. Ismail et al. [12] has introduced fast model which includes only three charge states (n-1,n,n+1). This mode is very fast in comparison with Quantum Transport software which includes about two hundred charge states. But in comparison with the proposed model when includes three charge states, our model is capture drain to source voltage = $2e/C_{\Sigma}$ but the other V_{ds}=e/C_{Σ}. Hasaneen et al. [13] has introduced an accurate model for the SET. This model solves steady state master equation to capture drain to source voltage up to $4e/C_{\Sigma}$ using ten states. However, using the proposed model five states are needed to capture the same range of V_{ds}. Finally, Amit Jain et al. [14] has introduced an accurate model for the SET. This model solves steady state master equation to capture drain to source voltage up to $6e/C_{\Sigma}$ using eleven states. However, using the proposed model seven states are needed to capture the same range of V_{ds}.

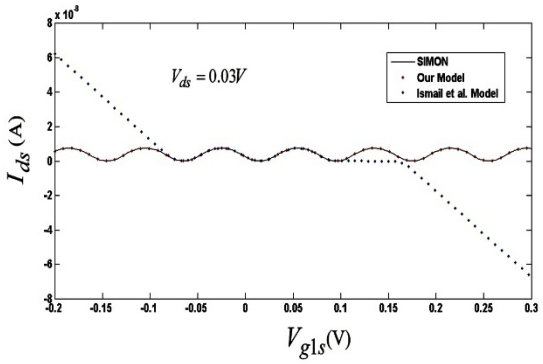

Fig. 9: Comparison between the proposed model and Ismail et al. model at C_g=2 aF, C_1=C_2=1aF, T=15k and R_1=R_2=1MΩ.

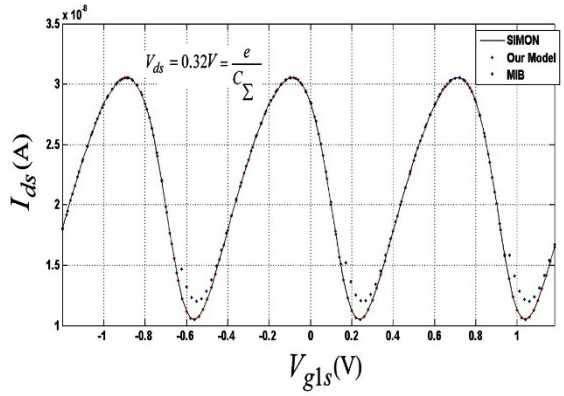

Fig. 10: Comparison between the proposed model and MIB model at Cg=0.2 aF, C1=C2=0.15aF, T=200k and R1=1MΩ, R2=5MΩ.

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The simulations in Figures 6(a), 6(b), 7, and 10 are repeated using MIB model [15], Hasaneen et al. model [13], Amit Jain et al. [14] and the proposed model. The Root Mean Square Percentage Error (RMSPE) between these models and SIMON results is calculated and summarized in Table 2. The results show that both the proposed, Amit Jain and Hasaneen's models maintain very small RMSPE, while MIB model shows wide range of deviation. Table 3 summarizes the comparison between the proposed model and previously reported models. The main advantages of the proposed model can be listed in the following points:

1) The proposed model is valid for both analog and digital applications as it captures unlimited range of V_{ds}.
2) The proposed model is valid for symmetric and asymmetric SET. The proposed model is faster than both Lientschnig's and Hasaneen's models.
3) The proposed model results show perfectly agree with SIMON results and the recursion relation model.
4) The proposed model is more simplified calculations, minimize current, power and improved speed for the numerical simulation.

4.1 Digital-to-Analog Converter (DAC) using the proposed SET model and MOS transistor

Figure 11 shows the basic schematic of an n-bit hybrid SET/MOS DAC circuit. It consist of two parts, the first part is a signal input capacitive array block, the second part is a Single Electron Transistor in series with depletion type NMOS (output block). The ratio of capacitor's values is $2^0:2^1:2^2:2^3:\ldots:2^n$ in the capacitance array. When an n-bit digital signal $D_0,D_1,D_2,\ldots\ldots D_{n-1}$ is applied to the capacitance array (first part), the output of the capacitance array is connected with the input of the output circuit (second part) which consists of SET in series with NMOS. The NMOS transistor M_1 acts as the load of SET, its gate is connected with the source. In this circuit Single Electron Transistor was used with one gate, this gate (G) acts as signal input end. The input gate of the SET and the source of NMOS are shorted in the output circuit (second part). The drain current of the SET oscillates periodically with the increase of input voltage signal at the input gate [16]. The analog voltage is used as output signal of the hybrid DAC circuit.

Table 2: Comparison of calculated RMSPE between MIB model [15], Hasaneen et al. model [13], Amit Jain et al. [14] and the proposed model.

			Root Mean Square Percentage Error (RMSPE)		
		MIB Model [15]	Amit Jain et al. [14]	Hasaneen et al. model [13]	The proposed model
Number of included states		4	11	10	5
Figure 6(a)	V_{ds} = 0.05V	0.12%	0.02%	0.02%	0.02%
	V_{ds} = 0.04V	0.46%	0.02%	0.02%	0.02%
Figure 6(b)	V_{ds} = 0.05V	0.27%	0.02%	0.02%	0.02%
	V_{ds} = 0.04V	1.16%	0.02%	0.02%	0.02%
Figure (7)	V_{gs} = 0.1V	0.24%	0.03%	0.03%	0.02%
	V_{gs} = 0.07V	0.03%	0.02%	0.02%	0.02%
	V_{gs} = 0.04V	0.05%	0.02%	0.02%	0.02%
Figure (10)	V_{ds} = 0.32V	7.52%	0.03%	0.03%	0.03%

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Table 3: Comparison between the proposed model and the previously reported models.

SET Model	Maximum V_{ds} range	Number of charge states	Validity to analog applications
Lientschnig et al. model [11]	Unlimited	11	Valid
Ismail et al. model [12]	e/C_{Σ}	3	Not valid
MIB model [15]	$3e/C_{\Sigma}$	4	Valid
Amit Jain et al. [14]	$6e/C_{\Sigma}$	11	Valid
Hasaneen et al. model [13]	$4e/C_{\Sigma}$	10	Valid
The proposed model	Unlimited	7	Valid

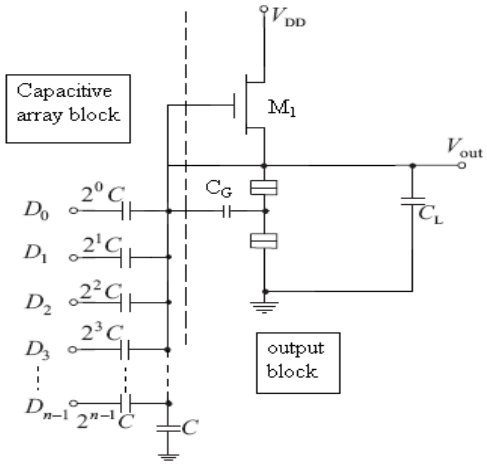

Fig. 11: Schematic of n-bit hybrid SET/MOS DAC circuit

Simulation results of 4-bit and 8-bit DAC circuits

This circuit is SET/MOS hybrid DAC circuit, which is difficult to simulate using the MOS circuit simulation method or the SET circuit simulation method separately. Therefore the proposed model using OrCAD Capture PSPICE program that is used in the circuit by one-gate SET simulation model. Compared with pure SET DAC circuit [17],[18], the proposed hybrid SET/MOS DAC uses fewer electronic components, which simplifies the structure of the circuit, increase the operating temperature, enhances the load capability and the signal output scope. Fig. 12 shows the simulation results waveform of 4-bit DAC circuit using Orcad Capture PSPICE. Compared with DAC circuit in [16]. The improved hybrid SET/MOS DAC uses fewer electronic components, simplifies the structure of the circuit, enhances the load capability and the signal output. The power dissipation of designed 4-bit DAC is 3.25E-11W,

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which is lower than the previous proposed SET/MOS DAC [16]. Table 4 shows a comparison between the previously reported DAC in [16] and the improved DAC. Fig. 13 shows the simulation results waveform of 8-bit DAC circuit using Orcad Capture PSPICE.

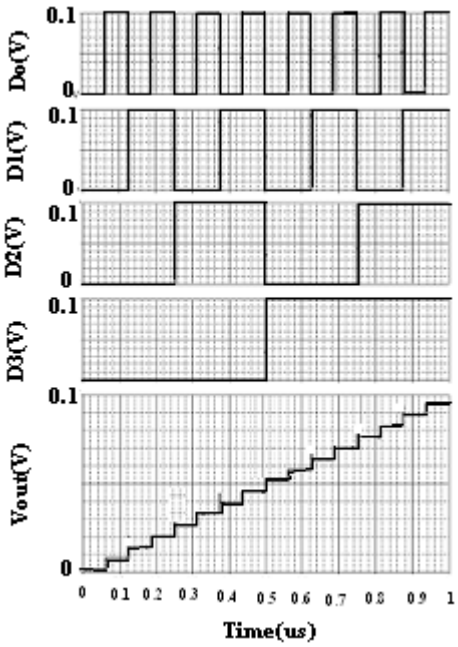

Fig. 12: PSPICE simulation results for the proposed 4-bit hybrid DAC.

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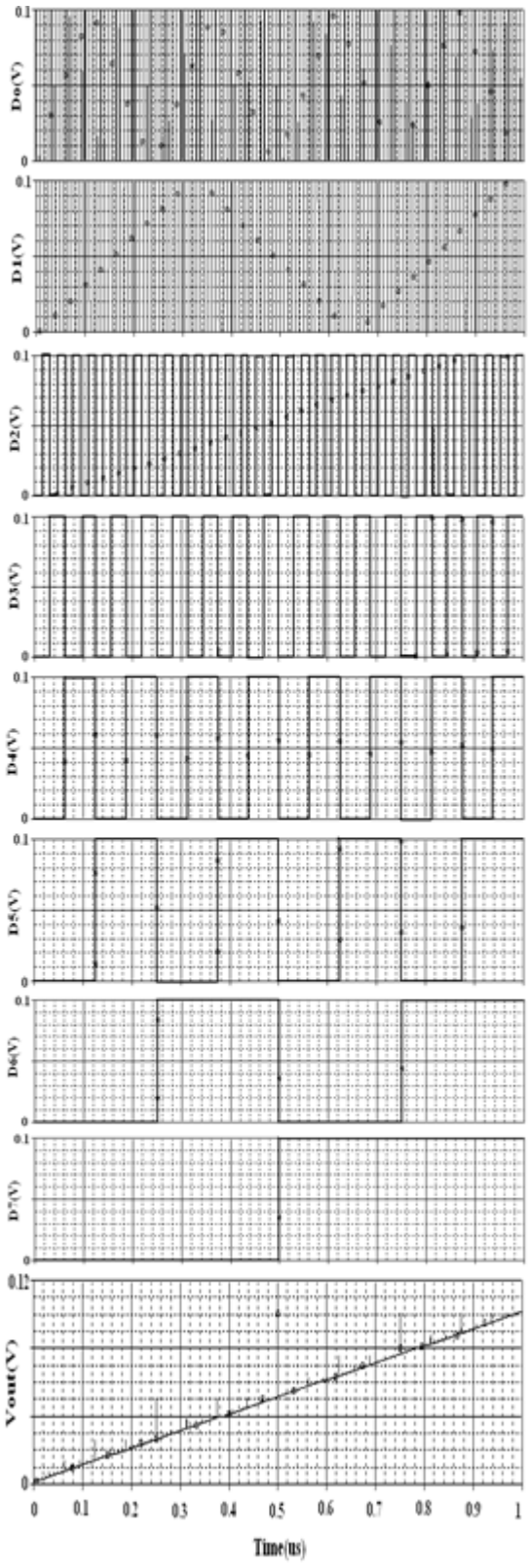

Fig. 13. PSPICE simulation results for the proposed 8-bit hybrid DAC

Table 4: Comparison between the previously reported DAC in [16] and the proposed DAC

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The simulation parameters	Hybrid 4-bit DAC [16]	Proposed DAC
Power dissipation	25.2E-11W	3.25E-11W
Capacitance Array Block (F)	C=1E-12F	C=10E-12F
Capacitive drive capability	several fFs	several hundreds of fFs=500fF
Temperature (K)	100K	20-1000K
Total job time	38.27Sec	15.86Sec
SET parameters	C_{G1}=1.8E-18F C_{G2}=0.64E-18F C_1= C_2=1E-19F R_1=R_2=2E6Ω	C_G=2E-18F C_1=C_2=1E-19F R_1=R_2=1E6Ω
NMOS parameters	M_1: L= 150nm W= 30nm Depletion type	M_1: L=150nm W=15nm V_{th}=-0.018V Depletion type

4.2 Analog-to-Digital Converter (ADC) using the proposed SET model and MOS transistor

Figure 15 shows the schematic of an n-bit hybrid SET/MOS ADC circuit. It consists of a capacitive divider and *n* Periodic Symmetric Function (PSF) with the same circuit parameters [19]. The PSF circuit is composed of two cascade circuits that are shown in Fig. 14. The first part is a SET in series with depletion type NMOS (the same as the output circuit of DAC), the second part is a SET in series with NMOS transistor. The ADC operation as follow: The analog input signal V_{in} is divided by the signal divider into n voltage signals ($V_{in}/2^i$, i= 0,1,2,….n-1). Then, the analog signals are converted into the corresponding binary output signal by the PSF units with the same circuit parameters. Fig. 16 shows the (V_{o1}-V_{in}) waveform of PSF at different temperature (5, 30, 50, 80, and 100K). From the figure as the temperature increase, the output of the first part V_{o1} become smoother.

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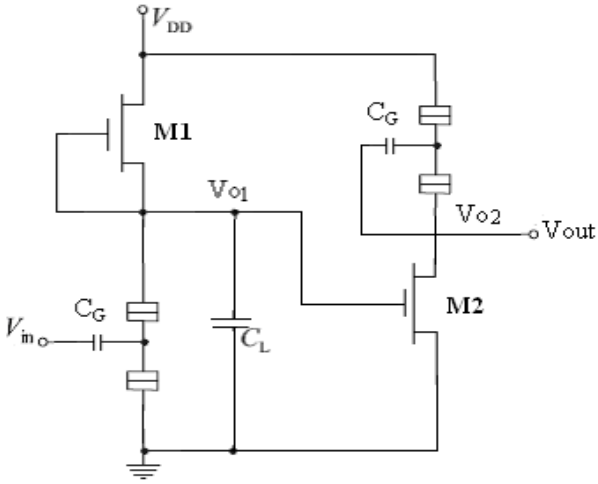

Fig. 14: Schematic of a SET/MOS Periodic Symmetric Function (PSF).

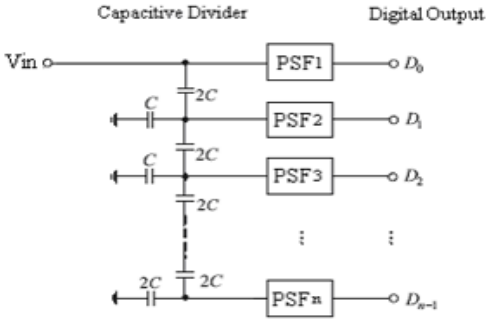

Fig. 15: Architecture for an n-bit ADC

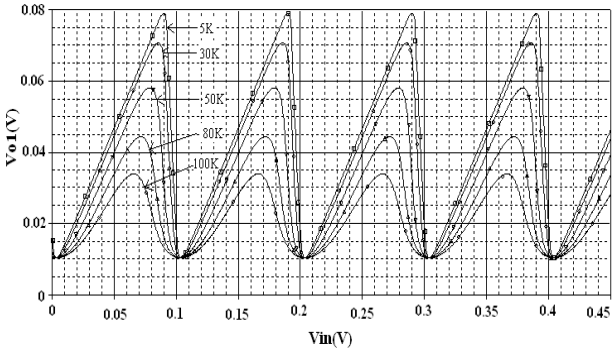

Fig. 16: The waveform of (V_{o1}-V_{in}) under different temperature

Simulation results of 3-bit ADC and 8-bit ADC circuits

Figure 17 shows the Voltage Transfer Characteristics of SET/MOS Periodic Symmetric Function (PSF) at 100K. Figure 18 show the simulation results of 3-bit ADC circuit using the PSPICE proposed model, the first waveform is the input ramp voltage, the rest of the waveforms show the digital output signal D_0, D_1 and D_2. Table 5 shows a comparison between the previously reported ADC in [16] and the proposed ADC. An 8-bit ADC circuit was simulated using Orcad Capture PSPICE. Compared with the previous proposed SET/MOS ADC [20], the proposed 3-bit ADC circuit has only one power supply and it can

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operate at higher temperature. Compared with the previous proposed SET-based ADC [21],[22],[23], the proposed hybrid SET/MOS ADC is enhanced in operate temperature from 0K~10K to144K, heightened the load capability and signal output scope.

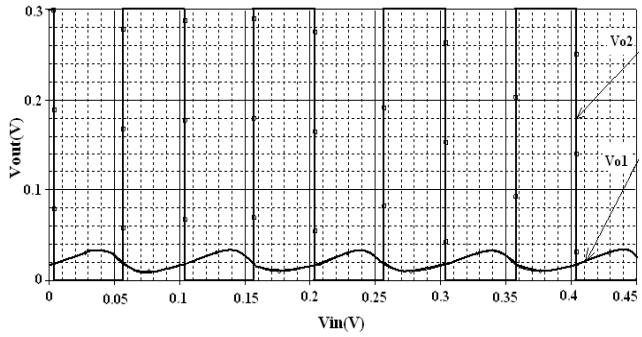

Fig. 17: Voltage Transfer Characteristics of Periodic Symmetric Function (PSF)

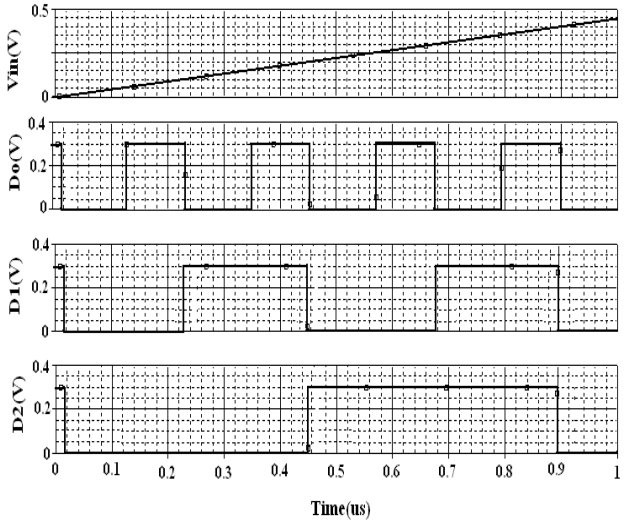

Fig. 18: Simulated waveform of 3-bit ADC Hybrid SET/MOS

Table 5: Comparison between the previously reported ADC in [16] and the proposed ADC

The simulation parameters	Hybrid 3-bit ADC [16]	proposed ADC
Power dissipation	5.88E-10W	2.92E-10W
Capacitance Array Block (F)	C=2E-15F	C=5E-15F
Capacitive drive capability	several fFs	several hundreds of fFs=500fF
Temperature (K)	100K	40-144K

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Total job time	277.66 Sec	30.44 Sec
SET parameters	C_{in}=1.6E-18 F C_{G2}=0.1E-18 F C_1=C_2=0.2E-18 R_1=R_2=8E6 Ω	C_G=1.6E-18 C_1=C_2= 2E-19 R_1=R_2=9E6Ω
NMOS parameters	NMOS parameters M_1: L=200 nm W=20 nm M_3: L=120 nm W=28 nm V_{th}=0.018 V PMOS parameters M_2: L=120 nm W=56 nm V_{th}= -0.482 V	Depletion type M_1:L=200 nm W=20 nm Enhancement M_2:L=120nm W=28nm V_{th}=0.018V

5. Conclusions

A new PSPICE model for the single electron transistor has been reported which is accurate and efficient for large range of bias voltage that is suitable for simulating circuits in hybrid SET/ MOS. The proposed model has been verified against the Monte Carlo simulator SIMON. The model was employed with MOSFET transistors to realize a multi-bit Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). The circuits performance can be compared with the pure SET circuits, the proposed converter circuits have been enhanced in the drive capability, signal swing of the output and the power dissipation. Compared with the other SET/MOS hybrid circuit, the implemented converter circuits have compact circuit structure, higher integration density, high speed, high load drivability, low current and low power dissipation.

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