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FULL LENGTH ARTICLE

A Novel Approach for Minimizing the Process Voltage Temperature Variation (PVT) Detector for Digital Converter Design

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ABSTRACT

Time-to-digital converters (TDCs) are vital components in digital circuitry, crucial for synchronization and precise measurement, demanding high resolution and accuracy. This brief introduces a novel TDC designed in order to reduce the impact of fluctuations in process, voltage, and temperature. A process voltage temperature detector using an extra delay line that is optimized for locking situations is incorporated into the suggested TDC to distinguish PVT corners effectively. Implemented in a 90-nm process, on-silicon measurements reveal impressive performance achieving 30-ps resolution.

Keywords: D-flip-flop (DFF) ▪ Process voltage and temperature (PVT) ▪ PVT corner detector ▪ Time-to-digital converter (TDC)

1. INTRODUCTION

Time-mode circuits, which encode analog information through the time difference between two digital signals, present a promising solution to the challenges in analog signal processing. Time-to-digital converters (TDCs) play a crucial role in these circuits, measuring time intervals and converting them into digital outputs. This functionality is essential in applications such as time-of-flight measurements, particle lifetime analysis, and especially in atomic studies. TDCs have been pivotal in high-energy physics and nuclear science, integrating into Analog-to-Digital Converters (ADCs), all-digital Phase-Locked Loops (PLLs), and digital converters to efficiently manage analog signals.

To achieve finer resolution, TDCs often employ techniques such as Vernier delay lines, time amplification, and multi-phase clocking. Vernier delay lines improve resolution by creating a minor difference between two delay lines, while time amplification involves stretching a minor interval to make it easier to measure. Multi-phase clocking enhances the measurement precision by using multiple clock phases to interpolate the time interval. Furthermore, advancements in semiconductor technology have enabled the development of TDCs with higher accuracy, lower power consumption, and smaller form factors, making them suitable for a wide range of applications beyond traditional domains. These advancements have broadened the scope of TDC usage to include medical imaging, LiDAR systems, and high-speed communication networks. The continuous innovation in TDC design and implementation is crucial for the advancement of modern electronics, where precise timing information is increasingly critical.

The proposed time to digital converter featuring an anti-process, voltage, and temperature variation mechanism is illustrated in Figure 1.

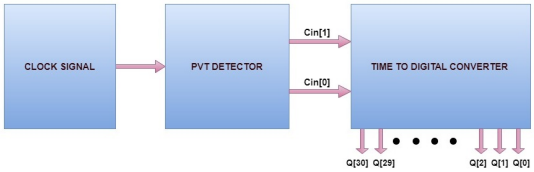

Figure 1. Time to digital converter diagram

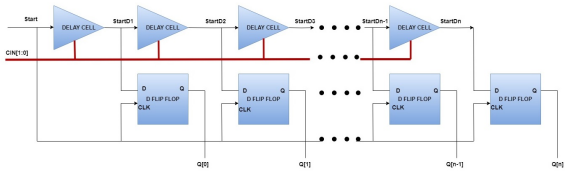

Figure 2. Block diagram of TDC.

The Digital Object Identifier for this work is in Figure 1, the proposed time to digital converter diagram includes a clock signal input fed into a PVT detector. This detector generates two random signals, CIN (1) and CIN (2), which are then inputted to the TDC converter. The TDC converter processes these signals to produce an output ranging from q (0) to q (30).

2. PROPOSED SYSTEM

The following are the main processes in processing a Time-to-Digital Converter (TDC), which is a component that converts the time interval between two occurrences into a digital assessment and is widely used in applications such as particle physics, time-of-flight measurements, and high-precision timing systems. The figure 2 representation of TDC block diagram.

2.1 Core Circuit

Time to digital Converter (TDC), which is the main component of the system, is constructed using the delay line structure shown in fig no 2. A "start" signal initiates the input at first, and it takes time T for it to reach the "stop" condition. Upon the cessation or approaching of the "stop" signal, the D flip-flop (DFF) output toggles, signifying a change from "0" to "1." The time "T" to be evaluated and transformed by this transition. The TDC timing diagram example, shown in fig no 3, shows the interval between "start" and "stop," which shows T in Equation (1). In this case, N represents the length of the thermometer code, and $\tau 1$ is the conclusion of every delay element.

$$T = N \cdot \tau_1 + \varepsilon \tag{1}$$

where ε denotes the faulty error [1]. The range (DR) is described as [n + 1] $\tau 1$, the 'n' denotes the delay elements. The schematic of the proposed Time to Digital Converter (TDC) given in Fig.4, includes two inverters. The first inverter receives the signal IN-TDC at its input and its output serves as the input to the second inverter. The result of the second inverter is labeled as OUT-TDC. The timing chart for TDC is shown in figure 3.

Additionally, a pull-down network consisting of three NMOS transistors, which are operated by inputs C<0>, C<1>, and VDD [2]. The PMOS transistors in the inverters have widths

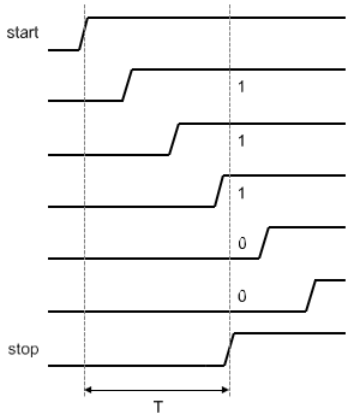

Figure 3. Timing Chart for TDC.

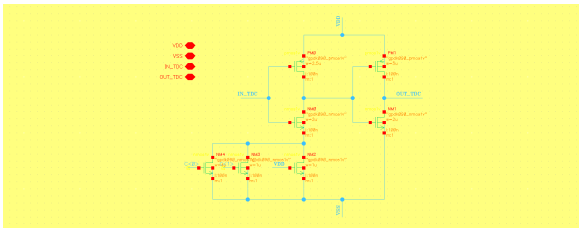

Figure 4. Schematic of TDC.

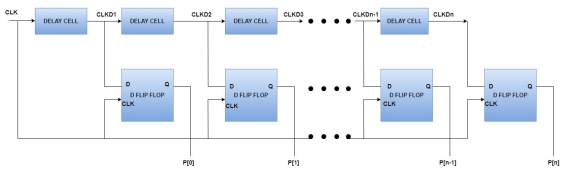

Figure 5. The detector's block diagram (PVT).

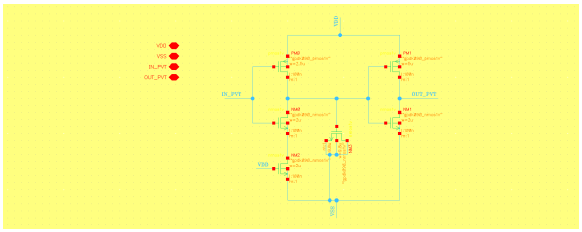

Figure 6. Implemented Schematic of Delay cell.

of 2.5μm and 5μm, while the NMOS transistors in the inverters have widths of 2μm each. The widths of the remaining NMOS transistors in pull-down network are 1μm.

As seen in the timing diagram, the measurement period until another event, the stop signal, halts the counting process. The distinction between the start and stop times determines the measured time interval, displayed as a digital value on the vertical diagram [3]. This digital output represents the precise time difference between the start and stop events with high resolution, vital for applications that call for precise time measurements.

In this study, with $\tau 1$ = 30ps and n = 31, the theoretical DR is 960 ps, it is worth noting that is notably influenced in this case, 90-nm CMOS required for circuit implementation on silicon. Further discussion on the design of delay cells is presented in subsequent process voltage and temperature detector and delay cell design [4]. Figure 4 shows the schematic diagram of the Time-to-Digital Converter (TDC).

An input of this cell, labeled as IN_PVT, undergoes inversion through an inverter stage. In this stage, the source of an NMOS transistor is connected to the drain of another NMOS

transistor, with the source of the latter linked to VSS (Ground). The gate of this second NMOS transistor is constantly supplied with VDD, ensuring its continuous activation [5]. This setup guarantees an unchanging function, where the input signal is inverted reliably. Figure 5 presents the block diagram of the PVT (Process, Voltage, and Temperature) detector.

The inverted output from the previous stage serves as the input to the gate terminal of another transistor. All other terminals of this NMOS transistor are tied to VSS. Subsequently, the output of this transistor is passed on to another inverter, where it serves as the input. Upon inversion in this subsequent stage, the resulting output is labeled as OUT_PVT. The NMOS devices employed in this configuration introduce delay to signal, facilitating the desired timing adjustments in the circuit. In the circuit diagram, the ratios of width to length (W/L) for the both PMOS and NMOS transistors [6]. This W/L ratio configuration ensures precise control over the delay characteristics, allowing designers to tailor the delay according to specific requirements and operating conditions. Figure 6 displays the implemented schematic of the delay cell used in the design.

2.1.1 Resistive Delay

When a component, usually a transistor or an interconnect, offers resistance, it causes a delay to be established in the circuit. This phenomenon is known as resistive delay. As signals go along the conductive channels of transistors or wires in digital circuits and run against resistance, resistive delay may manifest. A delay in the propagation is caused by this resistance, which prevents electric current from flowing.

Resistive delay can be a major factor in influencing the overall timing properties of delay cells or timing circuits. For instance, in a delay cell, a transistor's resistance—, which is frequently represented as an equivalent resistance—contributes to the total delay that a signal experiences as it passes through the transistor. In order to manage resistive delay and fine-tune the timing behavior of the circuit, designers can change the size (width and length) of resistor to optimize the interconnect arrangement. The delay cell, the NMOS transistor positioned at the source of the first inverter serves as the resistor component, generating resistive delay in the circuit.

2.1.2 Capacitive Delay

The delay that is injected into a circuit because of some components, like transistors or interconnects, having a high capacitance is known as capacitive delay. Capacitive delay occurs in digital circuits when signals interact with the circuitry's capacitive parts. The total capacitive load of a transistor is influenced by both the drain-to-source and gate-to-channel capacitances [7]. Likewise, the capacitive load is increased by the parasitic capacitance connected to wiring and interconnects. Conversely, the NMOS device situated at the output of the first inverter functions as the capacitor element. In this setup, the positive terminal of the capacitor is linked to the output, while the negative terminal connects to VSS, thereby creating capacitive delay. The delay cell's design is critically analyzed using Monte Carlo simulations, which provide insights into the circuit's robustness under various PVT conditions. By randomly selecting parameters within specified ranges, Monte Carlo analysis evaluates the statistical distribution of key performance metrics such as propagation delay and power consumption. Two specific outputs, Cin (1) and Cin (1) are chosen randomly from the PVT detector for further processing in the TDC converter block [8]. The simulations reveal that the delay cell can maintain consistent performance across a wide range of conditions, essential for ensuring the TDC's reliability. RC Delay.

2.1.3 RC Delay

When a signal propagates through a circuit because of both resistance (R) and capacitance (C), it is referred to as RC delay in digital circuits. In contrast to capacitance, which is derived from capacitive components in the circuit like transistor gates and interconnects that store electrical charge, resistance is caused by the conductive routes of transistors and interconnects, which obstruct the passage of electric current. After overcoming resistance and charging or discharging capacitors, signals travel through these resistive and capacitive devices with a delay. An RC time constant (τ) that controls the circuit's timing behavior is formed by multiplying resistance by capacitance, which results in resistor and capacitor delay. The combination of these resistor and capacitor elements produces a resistor and capacitor delay mechanism within the delay cell, crucial for regulating timing behavior and achieving precise control over signal propagation.

The PVT detector serves to continuously monitor the condition of integrated circuits (ICs) by leveraging the delay in digital cell propagation. Illustrated in fig no 5, the schematic depicts the arrangement of components within the process voltage detector. Fig no 6 showcases the delay cell unique to the process voltage detector, distinct from those within the time delay line [11]. Comprising PM0, NM0, PM1, and NM1, along with the always-on NM3 (functioning akin to a R) and capacitance developed in NM0, this delay cell constitutes an resistance capacitance delay. The "clk" input drives the process voltage detector, buffered by a chain of delay cells where each cell introduces a delay $\tau 2$. In this study, M = 31 delay cells are employed to generate CLKD1, CLKD2, ..., CLKM. The delay pulses are then latched by its corresponding D flip-flops (DFFs), triggered by the falling edge of the original "CLK" signal. The implementation of the process voltage detector in Figure 7 [9].

In the realm of designing the PVT detector and its accompanying delay cell for the Anti-PVT-Variation Low-Power Time-to-Digital Converter (TDC), monte carlo simulation emerges as an indispensable tool for assessing the circuit's resilience and dependability amidst diverse process, voltage, and temperature (PVT) fluctuations [10]. By randomly selecting two outputs, CIN (1) and CIN (2), from the PVT detector, monte carlo analysis enables a comprehensive exploration of the circuit's behavior across a spectrum of manufacturing tolerances and environmental scenarios [12]. This rigorous examination helps unveil potential challenges such as timing discrepancies or susceptibility to parameter variations, thereby facilitating iterative refinements in the design process to ensure consistent and precise functionality under varying operational conditions [13]. Monte carlo analysis gives the valuable insights into the statistical distribution of critical performance parameters, empowering designers to optimize the circuit for enhanced yield and efficiency while effectively addressing the impact of PVT variations [14-15].

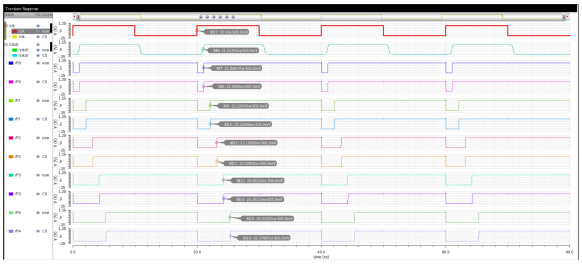

Figure 7. Monte Carlo analysis taken for the signals.

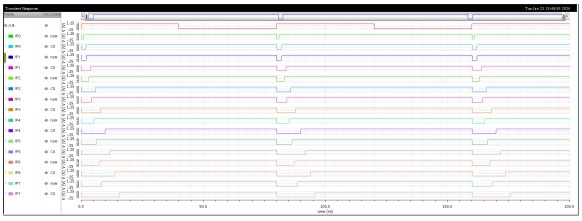

Figure 8. Extracted figure from the source document.

3. RESULTS AND DISCUSSION

Outputs of 22 and 28 of the process voltage and temperature detector's delay line are better thresholds for evenly classifying all edges into three corner groups: SLOW, TYPICAL, and RAPID, according to simulation as common locking case is seen in Fig.8, where x < y and the rising edge is latching by CLKDX and CLKDY produced by the PVT detector.

3.1 Robustness Using Monte Carlo Simulation

Monte Carlo models are utilized to meticulously test the delay cell's performance under a wide range of PVT conditions. This statistical approach involves running numerous simulations with random variations in process parameters, supply voltage, and temperature to obtain a comprehensive understanding of the delay cell's behavior.

Monte Carlo simulations involve randomly selecting two outputs, CIN (1) and CIN (2), from the PVT detector and feeding them into the TDC converter block. This block consists of two additional inverters and a pull-down network of three NMOS transistors located below the first inverter. The output of the first inverter in the TDC block serves as the input to the second inverter, and the final outputs are the TDC outputs. Figures 7, 8, 9, 10, 11 Illustrate Monte Carlo analysis results for the signals to evaluate statistical performance variations.

By analyzing the results of these simulations, designers can identify potential performance bottlenecks and ensure that the delay cell meets the required specifications across all possible manufacturing and operational scenarios. This process is crucial for achieving a reliable and accurate TDC. Analysis taken for the signals.

F

Figure 8. Monte Carlo analysis taken for the signals P(0)-P(7).

In this analysis, two specific outputs, CIN (1) and CIN (2), are randomly chosen from the PVT detector. These outputs are then sent to the TDC converter block, which comprises two additional inverters and a pull-down network made of three NMOS transistors beneath the first inverter. The output from the first inverter in the TDC block serves as the input to the second inverter, producing the final TDC outputs. This comprehensive approach allows for a detailed assessment of

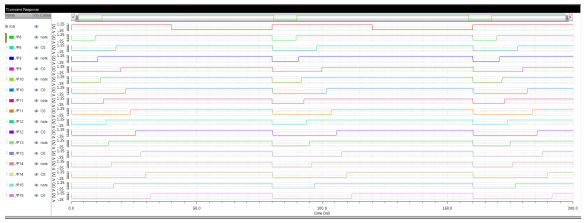

Figure 9. Monte Carlo analysis taken for the signals P (8) - P (15).

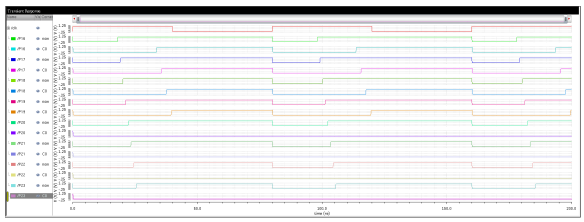

Figure 10. Monte Carlo analysis taken for the signals P (16)-P (23).

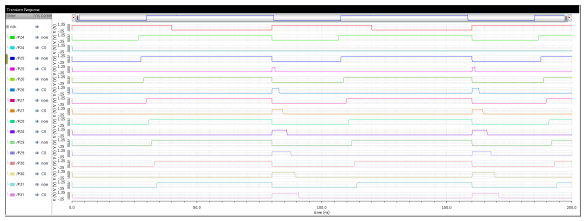

Figure 11. Monte Carlo analysis taken for the signals P (24)-P(31).

the delay cell's interaction within the larger TDC architecture

In the context of PVT analysis, Monte Carlo methods involve running simulations with randomized inputs within specified statistical distributions for parameters like voltage, temperature, and process variations.

Monte Carlo simulations played a crucial role in validating the design, providing insights into the statistical distribution of performance metrics and guiding the optimization process. The comprehensive analysis and iterative improvements resulted in a delay cell that meets the stringent requirements of high-precision digital circuits. Role of Montecarlo Simulations

3.2 Role of Montecarlo Simulations

Monte carlo simulations are employed to validate the design's robustness and performance under various PVT conditions. By randomly selecting parameters within defined ranges, monte carlo offers a statistical perspective on the delay cell's behavior, encompassing propagation delay, power consumption, and overall stability. This method is instrumental in identifying and mitigating potential design flaws, ensuring that the delay cell performs reliably across a wide range of conditions.

The subsequent outcomes for each PVT corner scenario are delineated as follows. A "Fast" PVT corner, characterized by shorter buffer delays, the receding edge of "CLK" aligns with the "high" levels of CLKD 22 and CLKD 28, resulting in "1 1" registration inside the relevant DFFs. It ought to be mentioned that these DFFs produce inverted outputs, which result in P (23) = 0 = CIN (0) and P (28) = 0 = CIN (1). In contrast, the dropping edge of "CLK" correlates with the "low" values of CLKD 22 and CLKD 28 for a "Slow" PVT corner where delays are lengthened, resulting in "0 0" registration in their respective DFFs. P [23] = 1 = CIN (0) and P (28) = 1 = CIN (1) are the outcomes of this arrangement. P (23) = 0 = CIN

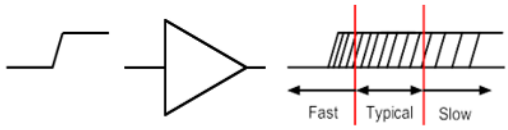

Figure 12. Delay Block of PVT.

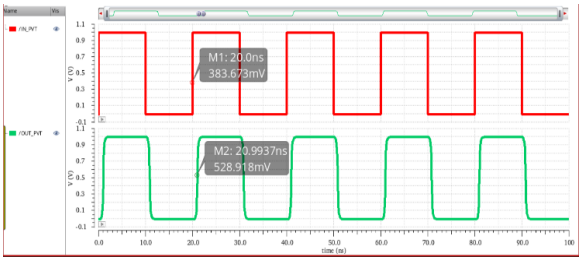

Figure 13. Delay Block of PVT detector [18], CIN 22, and CIN 28.

(0) and P (28) = 1 = CIN (0) are the results of the alignment of the falling edge of "CLK" with the "high" level of CLKD 22 and the "low" level of CLKD 28 in the case of a "Typical" PVT corner. Figure 12 depicts the delay block of the PVT detector.

Figure 13 compares the delay block of the PVT detector from this study with references [18], CIN 22, and CIN 28. The waveform analysis of delay block of the PVT detector is shown in figure 13.

3.3 TDC Core's Delay Cell

In figure 2, the inputs have control over the delay cells in the delay line. CIN (1) and CIN (0), directly receive outputs from process voltage and temperature detector to enable auto-adjustment of the delay [16]. The schematic representation of these delay cells within the time to digital Converter core is in figure4.

When operating in the slow mode CIN (1) and CIN (0) are 1 and 1, NM4 and NM3 transistors are activated to reduce the delay.

In the Typical mode, where CIN (1) and CIN (0) are 1 and 0, only NM4 transistor remains active, representing the standard operational condition.

In the Fast mode, CIN (1) and CIN (0) are 0 and 0, NM5 transistor is left conducting to increase the delay by sinking current. Core's Delay Cell

The aspect ratios of the pull-down NMOS transistors differ among NM4, NM5. The cause of this disparity is the requirement to manage sinking currents [17]. In the Typical mode, the baseline sinking current is established. For the Fast mode, this current is halved, while in the slow mode, it doubles [20-22]. Accordingly, the ratios of NM1, NM3, NM4, and NM5 are set at 02, 04, 01 to achieve the desired current-sinking ratios [19].

A 32-bit Phase-Voltage-Temperature (PVT) detector is an advanced monitoring system designed to make sure that optimal performance and reliability of integrated circuits. It meticulously tracks the phase of clock signals, voltage levels, and operating temperatures within a semiconductor device. Utilizing a Phase-Locked Loop (PLL), the detector synchronizes the system's clock with an external reference, ensuring minimal jitter and high-speed signal integrity [23]. Figure 14 represents the schematic diagram of the PVT detector designed for 32 bits.

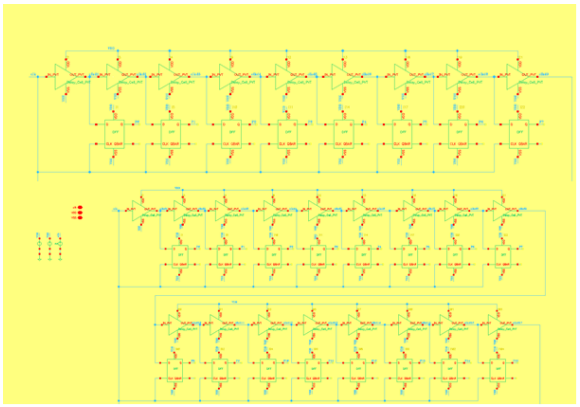

Figure 14. PVT detector schematic diagram for 32 bits.

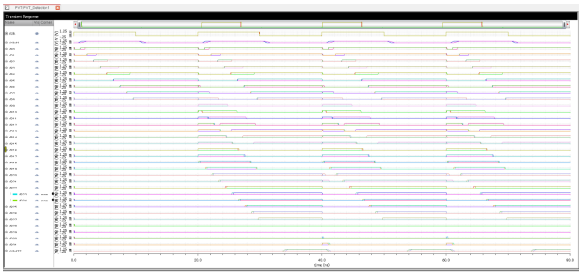

Figure 15. PVT with monte carlo analysis for 32 bits.

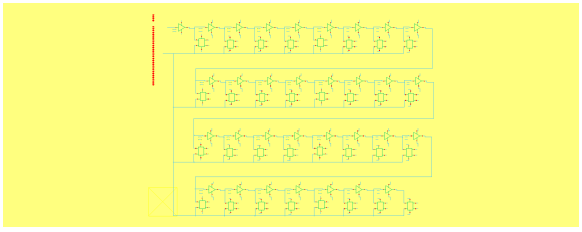

Figure 16. TDC detector schematic diagram for 32 bits, part 1.

A 32-bit Time-to-Digital Converter (TDC) is a highly precise electronic device utilized as a gauge the time difference between nanosecond or picosecond resolution. It is essential in applications such as high-energy physics experiments, medical imaging systems, and time-of-flight (ToF) measurements [24]. The TDC operates by converting the interval of time between two signals into a digital value, which is then processed by a 32-bit microcontroller or processor. This high bit-depth allows for extremely fine temporal resolution vital for applications needing extreme precision and accuracy. Figure 15 Demonstrates the Monte Carlo analysis results for the PVT detector with 32-bit implementation.

The TDC achieves this by using a mix of delay lines, phase detectors, and digital counters. Integration into a 32-bit system involves interfacing the TDC with fast and efficient communication protocols, such as SPI or parallel interfaces, ensuring rapid data transfer and minimal latency. Additionally, the system's firmware managing the TDC data, performing calibration, and compensating for any environmental variations to maintain measurement accuracy [25]. Overall, a 32-bit TDC applications demanding precise timing information, enabling advanced technological innovations and discoveries. Figure 16 shows the schematic diagram of the TDC detector for 32 bits.

Figure 17 Provides Monte Carlo analysis results for the 32-bit TDC detector.

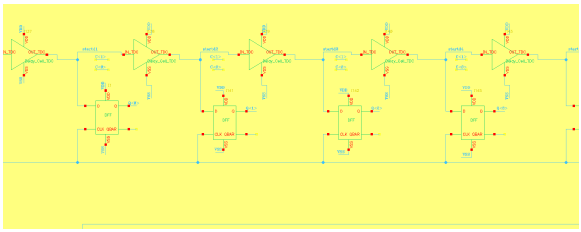

Figure 17. TDC detector schematic diagram for 32 bits, part 2.

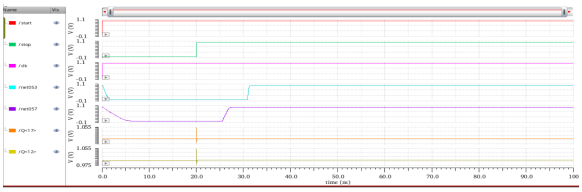

Figure 18. TDC with monte carlo analysis for 32 bits.

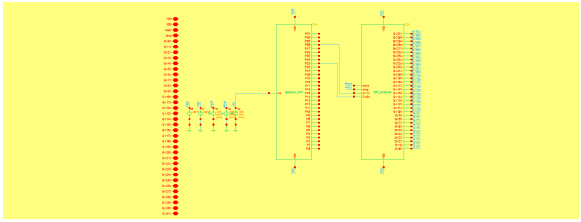

Figure 19. PVT detector with TDC for 32 bits

3.4 Overall Implementation

Integrating Time-to-Digital Converter (TDC) functionality with Process-Voltage-Temperature (PVT), monitoring can significantly enhance the precision and efficiency of time interval measurements in semiconductor devices. By incorporating TDC into the PVT monitoring system, the delay in measuring time intervals can be reduced due to several key factors.

Firstly, TDCs are designed to accurately measure minor differences with high resolution, often in the range of nanoseconds or even picoseconds. This feature enables accurate determination of timing events, crucial for applications like high-energy physics experiments, medical imaging systems, and time-of-flight measurements.

Implementing a comprehensive process voltage temperature (PVT) and time to digital Converter detectors into a 32-bit architecture significantly enhances the precision and reliability of advanced electronic systems. The PVT detector ensures the stability of the semiconductor device by continuously monitoring and adjusting the phase of clock signals, power supply voltage, and operating temperature.

This is achieved using a Phase-Locked Loop (PLL) for phase synchronization, Analog-to-Digital Converters (ADCs) and Power Management ICs (PMICs) for voltage regulation, and precise digital temperature sensors for thermal management. Meanwhile. The TDC counts the durations between events with high accuracy, utilizing delay lines, phase detectors, and digital counters to convert time differences into digital values. Both detectors interface with the 32-bit microcontroller through high-speed communication protocols like SPI or parallel interfaces, enabling rapid data transfer and real-time processing.

The microcontroller's firmware orchestrates the data from PVT and TDC detectors, performing essential tasks such as calibration, compensation for environmental variations, and

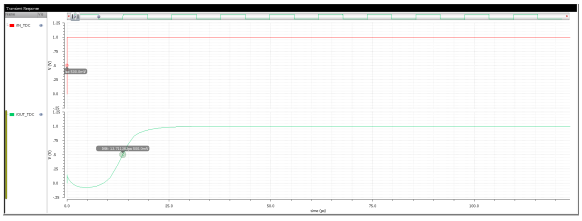

Figure 20. Variation in delay without detecting PVT

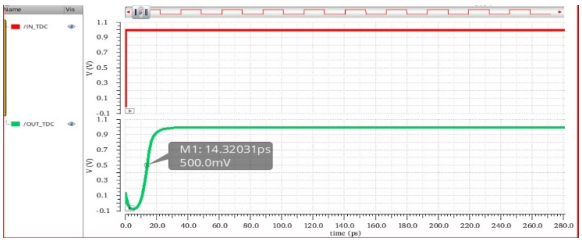

Figure 21. Difference in delay with PVT identification

dynamic system adjustments to optimize performance. This coordinated strategy not only ensures robust system stability and precision but also paves the way for advanced applications in fields like high-energy physics, medical imaging, and time-of-flight measurements, ultimately driving technological innovation and excellence. Figure 18 Integrates the PVT detector with the TDC for 32-bit configurations.

Furthermore, TDC and process voltage and temperature functionalities enable comprehensive data analysis and system optimization. Engineers can utilize Monte Carlo simulations and sensitivity analyses to understand how variations in phase, voltage, and temperature affect timing measurements. This all-encompassing strategy not only improves the precision of time interval measurements but also enhances overall system reliability and performance. Figure 19: Illustrates the variation in delay when the PVT is not detected.

3.5 Implementation and Measurement

Using the high-efficiency 90 nm CMOS process, the time to digital module with anti-PVT-variation technique is realized.

Process voltage temperature corners—Slow-Slow, Slow-Fast, Fast-Slow, and Fast-Fast as well as VDD levels between -15% and +15% and temperatures between 0°C and 100°C are covered by the simulation, this Monte Carlo method is run 1000 times. The variations before and after detection and self-adjustment are shown in Figures 10 and 11. The difference is lessened from 17 to 8.5 ps. with the implementation of process voltage and temperature detector with self-adjustment, a noteworthy 49.71% reduction.

In summary, integrating TDC with PVT monitoring reduces delay in time interval measurements by leveraging high-resolution timing capabilities, dynamic adjustment to PVT variations, and comprehensive system optimization. This integration is essential for advancing technological applications that demand precise timing information and reliable performance in diverse operating environments. Figure 20 highlights the difference in delay when PVT identification is applied.

It has been investigated how changes in temperature, process, and voltage affect circuit timing, with voltage variation found to dominate, having a four-fold impact compared to voltages ranging from 1.02V to 1.38V are utilized in the chips to verify insensitivity to PVT variations.

Process voltage and temperature corners— Slow-Slow, Slow-Fast, Fast-Slow, and Fast-Fast as well as VDD levels between -15% and +15% and temperatures between 0°C and 100°C are covered by the simulation. To make certain that the anti-PVT-variation design strong, this monte carlo method is run 1000 times.

Table 1. Performance comparison of different TDC

Performance metrics	ISSCS2015	ICCE2016	TCAS-II2018	MEJ2018	Proposed Work
Architecture	Vernier	DLL	Ring OSC	DUAL DLL	TDC
Process	65nm	65nm	130nm	180nm	90nm
Verification	Simulation	Simulation	Measurement	Measurement	Simulation
Resolution	6.15ps	2.0ps	43.2ps	15.0ps	30.0ps
DR	1260ps	1.0 μs	N/A	500ns	997ps
clock	40MHz	N/A	100MHz	100MHz	100MHz
Power	2.5mW	65 mW	1.72mW	75mW	2.22mW
Delay	24ps	N/A	22ps	19.0ps	14ps

The delay variations before and after using PVT detection and self-adjustment are shown in Figures 10 and 11. There is a decrease in delay variation from 17 to 8 ps. with the implementation of process voltage and temperature detector with self-adjustment, a noteworthy 49.71% reduction.

4. CONCLUSION

In conclusion, this research makes a significant advancement in time to digital converter design by incorporating a self-adjustment mechanism via process voltage and temperature detector. The integration of process voltage and temperature detection and the generation of corresponding PVT codes allow the system to dynamically select the optimal current-sinking path. This adaptive approach effectively counters delay drift, a common issue in TDC performance, thereby enhancing the stability and reliability of the system. The suggested time to digital design's ability to maintain consistent performance under varying PVT conditions is a testament to its robustness. Traditional TDC architectures often struggle with PVT variations, which can lead to inaccuracies and reduced reliability. By proactively addressing these variations, the proposed design ensures a higher level of precision and dependability. This is particularly important in applications where timing accuracy is critical. It not only improves the precision of time-to-digital conversion but also ensures the system's long-term reliability and stability. By improving the precision and reliability of time-to-digital conversion, the proposed design holds great promise for a wide range of applications, from high-speed data acquisition to precise time measurement in various advanced technological fields.

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